Data Sheet

SCP/DCP-124P

Single Freescale Power Architecture™ MPC7448 CompactPCI Single Board Computer

Features

- Single Freescale Power Architecture™ MPC7448 (AltiVec™ Technology- enhanced) CPU with:
  - 64KB L1 cache
  - 1MB internal L2 cache
  - ECC option on internal L2 cache
  - AltiVec-enabled e600 core (previously referred to as G4 core)
- High-performance Discovery III system controller
  - Dedicated CPU-to-SDRAM path reduces memory read latency
- 512MB of DDR SDRAM with ECC
- 256MB of contiguous direct-mapped Flash
  - Hardware Flash write protection jumper
- Permanent Alternate Boot Site (PABS) provides backup boot capability
- 128KB AutoStore nvSRAM with hardware write protection
- Two Ethernet interfaces (variant dependent):
  - Two 10/100Base-T to J2 connector or
  - Two Gigabit Ethernet (GbE) to J2 connector
- One 64-bit PMC on an independent PCI bus
  - 100MHz PCI-X capable
  - Optimized cooling of conduction-cooled PMCs
  - Full 64-bits of I/O routed to P2 as controlled impedance matched length signals
- One asynchronous RS-232 serial ports
- Up to two HDLC/SDLC-capable synch/asynch RS-232/422/485 serial channels with DMA support
- Up to eight LVTTL discretes software-configurable as input or output, with interrupt capability on inputs
- Up to eight RS-422/485 differential discretes (maximum of four inputs and four outputs), with interrupt capability on inputs, shared with RS422/485 lines
- One USB 2.0 port
- Four general-purpose 32-bit user timers
- Four general-purpose PCI/ SDRAM DMA controllers
- Six 32-bit OS timers
- Two avionics-style watchdog timers
- Real-time Clock (RTC)
- Two on-board temperature sensors
- CompactPCI (cPCI)
  - 32-bit, 33/66MHz cPCI bus with support for 3.3V and 5V VIO
  - Operates in a peripheral only mode
- Uses backplane +5V and 3.3V
- Backplane 3.3V, 5V, and +/-12V are routed to the PMC sites
- Occupies single .8" slot in all configurations
- Optimized conduction-cooling with TherMax™ thermal frame and direct processor shunts

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ABOVE & BEYOND

CURTISS WRIGHT Controls
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- Comprehensive Ethernet-capable Foundation Firmware with
  - Debug monitor with system exerciser functions
  - Power-up BIT (PBIT)
  - Embedded Non-volatile Memory Programmer (NVMP)
  - Support for warm boot/cold boot determination
  - SecureErase Utility provides users with a convenient means to erase all non-volatile memory elements for board information security purposes
- VxWorks®/Tornado™ integration:
  - Tornado 2.2.x and Workbench 2.x
  - Full suite of drivers for hardware features
  - Run-time BIT libraries for Initiated and Continuous BIT
  - Yellow Dog Linux, Denex ELDK Linux and Wind River Linux
- Continuum Vector AltiVec-optimized DSP library
- Available in a range of ruggedization levels, both air- and conduction-cooled

Overview

Using the Freescale Power Architecture MC7448 processors with AltiVec technology and up to 1GB of state-of-the art DDR1 SDRAM, the SCP/DCP-124P represents the latest advancement in functionality and performance for rugged 3U cPCI Single Board Computers (SBC). The SCP/DCP-124P has been designed to complement the SCP/DCP-124 with a PICMG 2.3 compatible pinout providing a full 64-bits of PMCIO on the P2 as a peripheral only card. With a 64-bit PMC site supporting 100MHz PCI-X, and an innovative complement of I/O capability such as GbE, up to 3 serial ports, and one USB 2.0 port, the SCP/DCP-124P satisfies the most demanding requirements of 3U embedded cPCI computing applications. Available in a full range of environmental build grades the SCP/DCP-124P is targeted to the challenging data- and digital signal-processing needs of tactical aircraft, armored vehicles and harsh environment naval systems.

Powerful Core Architecture

Figure 1 illustrates the core processing architecture of the SCP/DCP-124P. The powerful MPC7448 processors connect via the MPX bus to the advanced GT-64460 Discovery™ III system controller. The Discovery III system controller bridges the MPX bus of the processor to the DDR1 SDRAM bus, two 64-bit PCI busses one of which is used to implement the cPCI bus, and a high-performance device bus on which the Flash EPROM and non-PCI peripherals are found. The powerful crossbar fabric internal to the Discovery III device allows for concurrent data transfers to take place on the various busses of the SCP/DCP-124P. Examples of data transfers that can occur concurrently on the SCP/DCP-124P include:

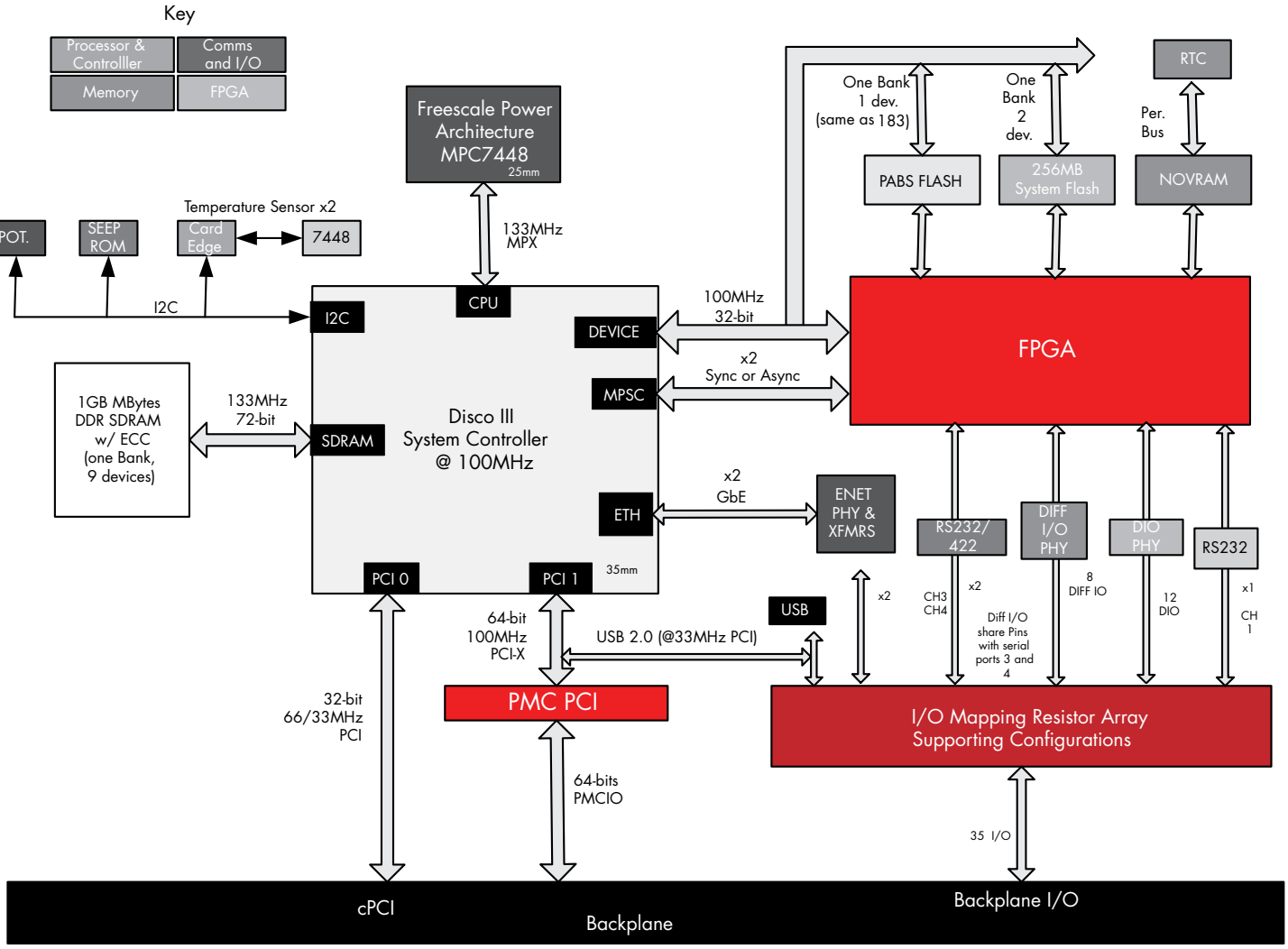
- Processor accesses to Flash concurrent with PCI-SDRAM transfers on either PCI bus
- Processor accesses to one PCI bus concurrent with PCI-SDRAM transfers on the other PCI bus
- Processor accesses to on-chip peripherals (Ethernet and serial ports) concurrent with PCI-SDRAM transfers on either PCI bus

The SCP/DCP-124P provides hardware-enforced cache coherency with respect to accesses to SDRAM from PCI and bus-mastering peripherals, freeing driver software developers from the complexity of managing cache coherency in software. For applications requiring the highest possible PCI-SDRAM performance, hardware-enforced cache coherency can be disabled.

The core functions FPGA is a Spartan-3 1000 device that implements a number of important SCP/DCP-124P features including asynchronous serial ports, interrupt control, system timers, watchdog timers, TTL discrete I/O and differential discrete I/O control registers. In addition, the core functions FPGA bridges the Discovery device bus to the Flash array and to a peripheral bus that interfaces to the RTC and nvSRAM. To increase the serviceability of the SCP/DCP-124P over the long life cycles of the military/aerospace programs for which it is designed, the core functions FPGA is In-System Programmable (ISP) and can be reprogrammed in the field.

PCI bus 1 is a 64-bit, 100MHz-capable PCI-X bus that is shared by the PMC site and the USB device. The PMC site is capable of operating in PCI-X mode up to 100MHz if the USB is not used. If USB is used, the site is limited to 33MHz PCI. Offering a peak PCI transfer rate up to 800MB/s, the PMC site has the necessary bandwidth to support high-performance PMC modules such as Fibre Channel NICs, graphics controllers, fabric interfaces, and custom high-speed devices. Also located on the PCI bus 1 is the USB controller which can be disabled when maximum PCI performance is required.

Figure 1: SCP/DCP-124P Core Processing Architecture



Discovery III Controller Delivers Full Potential of PowerPC MPX Bus

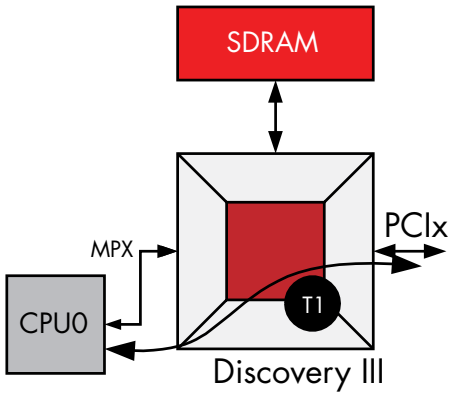
The 124P's Discovery III system controller provides optimum support for the PowerPC's advanced MPX bus interface providing the following performance features:

- Split transactions, illustrated in Figure 2, allows faster accesses such as to DDR SDRAM to complete in advance of an access to a slower device such as Flash or a PCI peripheral that was initiated first
- Address streaming; no dead cycles between consecutive address tenures driven by the same device
- Data streaming, no dead cycles between consecutive data phases driven by the same device
- A direct path between the MPX bus and system memory, which significantly reduces memory-read latency

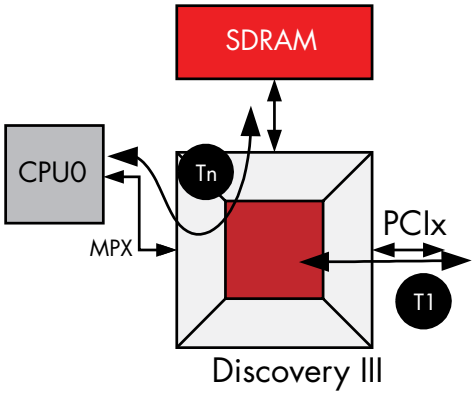
Support for the split transaction feature of the PowerPC's MPX bus allows the Discovery III system controller to provide data from high-speed targets such as SDRAM between the address and data phases of a transaction targeting a lower-speed peripheral.

Figure 2: Split Transaction Feature Support

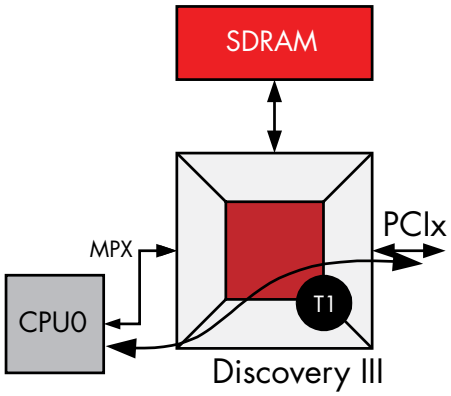
CPU0 initiates transaction T1 to a slower target such as a PCI peripheral.



While transaction T1 is in process on the PCI bus, one or more transactions, Tn, to a faster target such as SDRAM can take place



When data from the PCI peripheral is available, it is driven onto the MPX bus.





Flexible I/O

Table 1 illustrates the SCP/DCP-124P's variant dependent feature-rich I/O subsystem. I/O features integral to the SCP/DCP-124P include cPCI, one RS-232 ports, up to two GbEs, one USB 2.0 port, 2 RS232/RS422/485 ports or 8-bits of differential DIO, up to 8-bits of discrete DIO, card reset input. The I/O in this table represent those to be offered in standard product configurations. Other configurations of I/O are possible as customer specific variants.

Table 1: SCP/DCP-124P Flexible I/O

Mode	Fast Ethernet	GbE	RS-232	RS-422/485	USB 2.0	DIO	PMC I/O
Mode 3	-	2	1	2 (async only)	1	1	64
Mode 4	2	-	1	2 sync capable	1	1	64

Designed for Harsh Environments

To cost-effectively address a diverse range of military/aerospace applications, the SCP/DCP-124P is available in a range of ruggedization levels, both air- and conduction-cooled. All versions are functionally identical, with air-cooled versions (SCP) available in Curtiss-Wright ruggedization levels 0 and 100, and conduction-cooled versions (DCP) in levels 100 and 200. Curtiss-Wright's standard ruggedization guidelines define the environmental tolerance of each ruggedization level (see Curtiss-Wright Ruggedization Guidelines factsheet for more information).

Enhanced Thermal Management for Conduction-cooled Applications

For those demanding application environments that require conduction-cooling, the SCP/DCP-124P uses a combination of thermal management layers within the Printed Wiring Board (PWB) and an aluminum thermal frame that provides a cooling path for the PMC site and for high-power components such as the processor, and bridge device.

The DCP-124P thermal frame employs a number of innovative design techniques to keep the temperature rise of the electronic components to a minimum, thus increasing the long-term reliability of the product:

- Provision of both primary and secondary thermal interfaces on PMC site
- Mid-plane thermal shunts for PMC site
- TherMax design approach

Mid-plane Thermal Shunts for PMCs

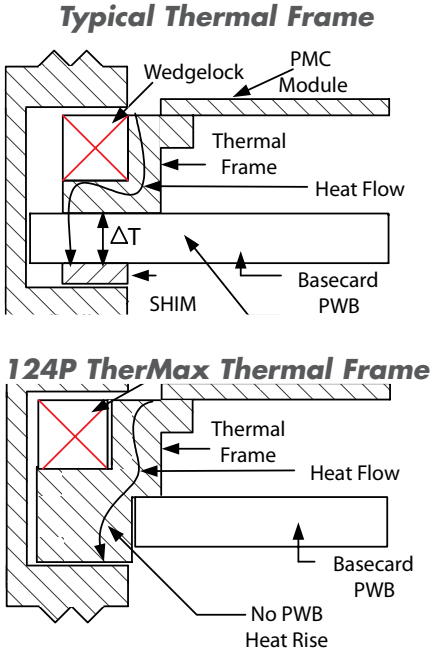
To optimize the conduction-cooling of high-performance, high-power PMC modules such as graphics or networking PMCs, the DCP-124P thermal frame incorporates mid-plane thermal shunts for the PMC sites. High-power PMCs can include a mating cooling surface on the PMC module to contact the mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed PMC modules can significantly lower the heat rise from the DCP-124P card edge to the PMC components. The mid-plane thermal shunt does not impinge on the VITA 20- allowed component height.

TherMax™-style Thermal Frame

A TherMax Thermal Frame provides an unbroken metallic path from the PMC sites and shunted components to the back-side cooling surface of the card therefore minimizing the temperature rise to these devices. In comparison, a typical thermal frame simply sits on top of the PWB and forces heat to flow through the PWB which has a high-thermal resistance compared to aluminum.

Figure 3: TherMax Diagram

A TherMax thermal frame eliminates the PWB heat rise inherent in a standard thermal frame



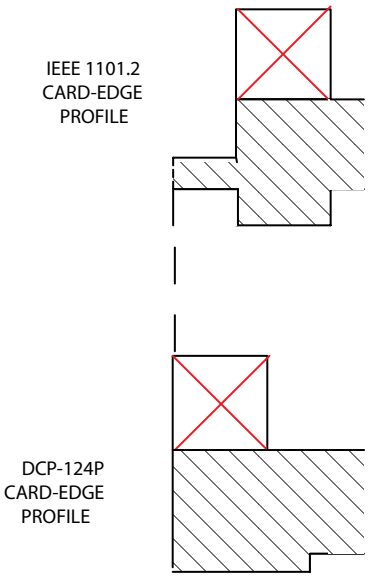


Full-width Thermal Interface to Back-side Slot Wall

To minimize the temperature rise from the mating slot wall of conduction-cooled enclosures to the back-side thermal interface region of the DCP-124P, the DCP-124P thermal frame maximizes the thermal interface area by extending the frame to the full width of the card, as illustrated in Figure 4. This deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in standard air-cooled chassis, has the benefit of lower card operating temperatures and increased long-term reliability. During test and integration activities where it may be desirable to install a conduction-cooled DCP-124P into an air-cooled card-cage, this can normally be accomplished simply by removing the card guides.

Figure 4: Card-edge profile deviates from IEEE 1101.2

DCP-124P Card-Edge Profile is Optimized to Provide a Full-width Thermal Interface to the Back-side Slot Wall



Advanced MPC7448 Processor CPU

The SCP/DCP-124P is equipped with the high-performance MPC7448 processor, advanced fourth generation members of Freescale's broad family of PowerPC family of 32/64-bit RISC microprocessors. Developed for a wide range of embedded computing applications, the MPC7448 provides industry-leading performance per watt. The SCP/DCP-124P MPC7448 processor runs at 1.0GHz or 1.2GHz. It has been designed such that Dynamic Frequency Shifting (DFS) of a divide by two and by four is supported when operating at 1.2GHz.

The MPC7448 processor incorporates Freescale's powerful AltiVec technology, which enhances the PowerPC architecture through the addition of a 128-bit vector execution unit. The vector unit provides for highly parallel operations, allowing for the simultaneous execution of up to 16 integer operations or eight floating point operations per clock cycle.

Table 2: CPU Performance

Processor	MPC7448 @ 1000MHz	MPC7448 @ 1.2GHz
Dhrystone 2.1 MIPS	2310	2773

Notes:
1. Extrapolated from MPC7448 data sheet

Powerful Interrupt Mapping Logic

Through a combination of the Discovery III system controller and logic implemented in the core functions FPGA, the SCP/DCP-124P allows the hardware to adapt to the needs of the software by providing a means to route all interrupts sources (PMCs, cPCI, PCI, peripherals, etc.) to the processor.

Up to 1GB of Dual Data Rate (DDR) SDRAM

The memory options for the SCP/DCP-124P include 512MB or 1GB of high-performance Dual Data Rate (DDR1) SDRAM. To preserve data integrity, the SDRAM is provided with Error Checking and Correcting (ECC) circuitry that detects and corrects all single-bit data errors, detects all double bit errors, and detects all 3 and 4-bit errors within the same nibble. With ECC enabled, the instantaneous peak data transfer rate to the DDR SDRAM is 2.0GB/s.

The DDR SDRAM is accessible from the processor, the PCI and cPCI bus.



256MB of Flash Memory

The SCP/DCP-124P implements up to 256MB of Flash memory. The SCP/DCP-124P's Flash is contiguous, directly-accessible, high-speed Flash memory using AMD S29GL01GP devices. The Flash will retain data for 20 years at +85°C. Note: these figures assume the sector the data is in has less than 1,000 erase cycles. The data retention drops as erase cycle count increases. After 10,000 cycles, data retention is for 10 years. After 100,000 cycles, data corruption will likely be noticeable in one year.

Read performance of the Flash array is optimized in order to minimize system boot-up time for applications such as avionics mission computers where fast restarts after power interruptions are critical, and execution directly from Flash without first cross loading to SDRAM is advantageous. Optimizations include:

- 32-bit wide Flash array
- 100MHz device bus operation
- Support for burst reads at 30 nsec.

For absolute security against inadvertent Flash programming or corruption, a hardware jumper is provided to disable the write enable line to the Flash devices. Cards are configured for shipment with Flash reprogramming enabled in hardware.

Flash memory is reprogrammable on-board using Curtiss-Wright's NVMP utility embedded into the standard foundation firmware.

Permanent Alternate Boot Site (PABS)

PABS provides a backup boot capability in the event that the Foundation Firmware in the main Flash becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. PABS provides users with a convenient mechanism to recover from corruption of the main Flash without removing the card from the system in which it is installed. With the setting of a on-board jumper, the SCP/DCP-124P will boot from PABS and run a version of Curtiss-Wright's standard Foundation Firmware that will allow user's to reinstall the standard firmware load.

256KB High-speed SRAM

Incorporated into the Discovery III system controller, the SCP/DCP-124P provides 256KB of high-speed SRAM directly on the processor's MPX bus. While useful as a general-purpose high-performance memory area that off-loads traffic to SDRAM, the high-speed SRAM is particularly beneficial for holding descriptors for Discovery III peripheral devices, allowing DMA units to simultaneously access data from SDRAM while descriptors are accessed from the SRAM.

128KB of AutoStore nvSRAM

A Simtek 14CA8N 45nsec. AutoStore nvSRAM provides fast, non-volatile storage of mission state data that must not be lost when power is removed. During normal operation, application software reads and writes the AutoStore nvSRAM just like standard SRAM, with no special programming algorithm required. Upon detecting a power loss on the +3.3V rail, an AutoStore cycle is performed and all 128KB are automatically transferred from the on-chip SRAM to the on-chip EEPROM using energy stored in an on-board capacitor. At the next power-up a recall cycle is performed to transfer the EEPROM contents back to the SRAM, where the application code can now utilize the stored data to continue normal operation. The number of recall cycles is unlimited: the maximum number of store cycles is 1,000,000 and the data retention period is 100 years.

For security against inadvertent writes to nvSRAM, a hardware jumper is provided to disable the write enable line to the device. Cards are configured for shipment with nvSRAM programming enabled in hardware.

Two Ethernet Interfaces

The SCP/DCP-124P is equipped with up to two 10/100/1000Base-T Ethernets, variant dependent, both implemented within the Discovery III system controller device. In the mode 3 variant, the SCP/DCP-124P implements them as 2GbE interfaces, while in the mode 4 variant, these are implemented as two 10/100Base-T fast Ethernets.

The Discovery III Ethernet controllers integrate a number of features designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for jumbo packets up to 9KB, efficient buffer management schemes, checksum calculation for IP, TCP, and UDP, and interrupt coalescence.

One RS-232 Serial Ports

Serial channel 1 is a RS-232 serial ports implemented with a 16550- based controller built into the core functions FPGA. A base clock of 36.864MHz allows for all standard asynchronous baud rates from 300baud to 115.2Kbaud. The baud rate of the port can be set independently. The DSR signal on serial channel is used as a cable detect signal to force the card to boot into the general purpose monitor of the foundation firmware.

Option for Up to 2 RS-232/422/485 Serial Ports

Up to a total of 2 asynchronous- and synchronous-capable RS-232/422/485 ports are available on the SCP/DCP-124P.

Serial channels 3 and 4 are implemented with the Discovery III's Multi-Protocol Serial Controllers (MPSC). These powerful serial controllers handle standard asynchronous and synchronous HDLC/SDLC modes, and in addition provide a transparent mode. In synchronous mode a full range of data encoding schemes are supported (NRZ, NRZI Mark, NRZI Space, FM0, FM1, Manchester, and Differential Manchester). Based on an input clock of 133MHz, all standard asynchronous baud rates up to 115.2Kbaud are provided as well as synchronous bit rates up to 5Mbits/s for NRZ clock mode, 2.5Mbits/s for clock-encoded modes (FM0, FM1, etc.). The Discovery III MPSC ports are equipped with dedicated DMA controllers to off-load the processors from handling serial data traffic to and from the controllers.

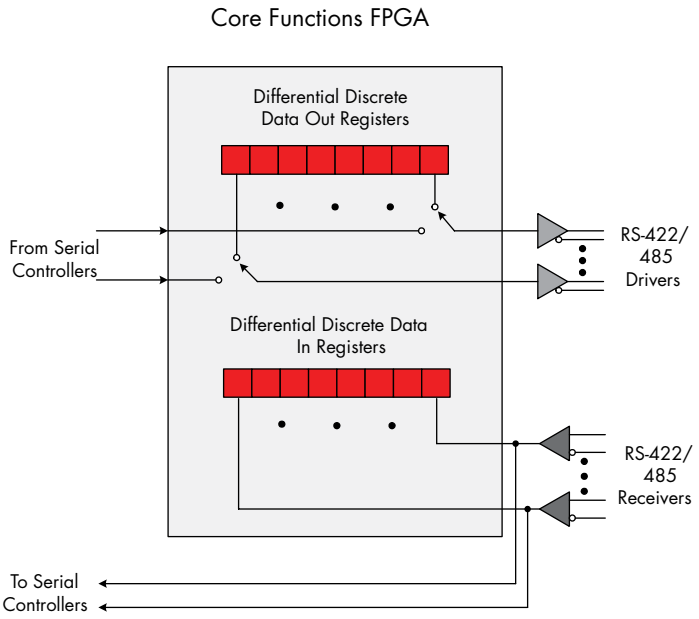
The choice of physical level (RS-232 or RS-422/485) for the MPSC serial channels is software selectable on a per-channel basis via a control register within the core functions FPGA.

See Differential Discrete I/O below for information on how the SCP/DCP-124P provides the capability to control each of the RS-422/485 drivers and receivers as differential-mode discrete signals for use as serial control signals or general purpose I/O.

Up to 8-bits of Differential Discrete Digital I/O

The SCP/DCP-124P provides the capability to control each of the RS-422/485 drivers and receivers as differential-mode discrete signals via registers in the core functions FPGA providing up to four differential-mode discrete inputs and up to four differential-mode discrete outputs depending on the variant. This allows flexibility in how the drivers and receivers are used. The choice of whether the drivers and receivers are attached to serial ports or used as discrete differential I/O is software selectable on a per-serial channel basis. When configured as discrete differential I/O, the drivers and receivers can be used as general-purpose differential-mode control signals unrelated to serial I/O requirements. Differential discrete inputs can generate an interrupt upon a change of state, with programmable edge direction. Note that if the serial channel physical levels are set to RS-232, then discrete digital I/O at RS-232 levels is obtained.

Figure 5: Discrete Differential I/O Option for Discrete Control of RS-422/485 Drivers and Receivers





One USB 2.0 Port

The SCP/DCP-124P incorporates an NEC uPD720100 or NEC uPD720101F (variant dependent) to provide one USB 2.0-capable port on a 32-bit, 33MHz PCI 2.2-compatible device. A port can handle high-speed (480MB/s), full-speed (12MB/s), and low-speed (1.5MB/s) operation. When operating at low- speed or full-speed, a port is managed by independent OHCI-compliant controllers internal to the device. One OHCI-compliant controller manages the port operating in high-speed mode. The USB port is accessible on the J2 connector only and is variant dependent. The port provides a current limited +5V output to power to low and high-power USB devices such as keyboards.

The NEC uPD720100 shares the PMC PCI bus. The NEC uPD720100 can be enabled or disabled through the use of a user selectable jumper. When enabled, the PCI bus 1 is limited to run at 33MHz PCI. If the device is disabled (i.e. not used), PCI bus 1 (hosting the PMC) can run at speeds up to 100MHz PCI-X.

8-bits of LVTTL Discrete Digital I/O

The SCP/DCP-124P optionally provides up to 8-bits of LVTTL compatible discrete digital I/O variant dependent (standard product is four). Each bit is individually programmable as an input or output. In addition, each bit when configured as an input is capable of generating an interrupt upon a change of state, with the edge direction (high-to-low, low-to-high) also being programmable. Each bit has a 10K pull-up resistor to 5V. Output drive current is 24 mA.

Real-time Clock (RTC)

A Maxim/Dallas Semiconductor DS1501 RTC chip provides the RTC function. It contains registers for century, year, month, day, hours, minutes, and seconds. The RTC is capable of generating alarm interrupts. The RTC draws its power from the standard +3.3V input during normal operation.

Extensive Timing Resources

The SCP/DCP-124P provides a large number of timing resources to facilitate precise timing and control of system events. The list of available timers is given in Table 3.

Avionics Watchdog Timers

The SCP/DCP-124P provides two watchdog timers. Each watchdog timer is a presettable downcounter with a resolution of 1 usec. Time periods from 1 usec to 16 seconds can be programmed. Initialization software can select whether a watchdog exception event causes an interrupt or a card reset. Once enabled to cause a reset, the watchdog cannot be disabled. A watchdog time-out log bit tells start-up code whether the last card reset was due to a watchdog exception.

The watchdog timer can be used in two ways. Used as a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in “Avionics” mode whereby a minimum interval between writes to the watchdog register is also enforced, i.e., writing to the watchdog register either too soon or too late causes an exception event. For added robustness the watchdog is run off an independent clock source to the CPU clock.

Table 3: Table of SCP/DCP-124P Timing Resources

Timer Facility	Implementation	Type	Size	Tick Rate/ Period	Maximum Duration
PowerPC Time Base Register	CPU	Free running counter	64-bit	33.33MHz/30.0 nsec.	17,549 years
PowerPC Decrementer	CPU	Presettable, readable downcounter	32-bit	33.33MHz/30.0 nsec.	128.8 sec.
General Purpose #0-3	Discovery III	Presettable, readable downcounter with autoreload or stop options	32-bit	133.33MHz/7.5 nsec.	32.2 sec.
RTC Alarm Interrupt	Real-time clock	Alarm interrupt	-	Specific day, hour, minute, and second	-
Watchdog Timers (x2)	Core Functions, FPGA	Presettable, readable downcounter with interrupt or reset on terminal count	24-bit	1MHz/1 usec.	16.77 sec
System Timers #1-6	Core Functions, FPGA	Presettable, readable, downcounters with interrupt on terminal count	32-bit	50MHz/20 nsec.	85.9 sec.

Four General Purpose DMA Controllers

Four DMA controllers provided by the Discovery III bridge chip are available for general purpose use. The four general purpose DMA controllers can be used for transferring blocks of data between the SDRAM, Flash memory, device bus peripherals, and the PCI busses without loading down the PowerPC CPU. The general purpose DMA controllers are capable of sustaining burst transfers using the full 64-bit width of the PCI bus. Advanced features include DMA chaining and the ability to schedule DMA transfers via a general-purpose timer.

CompactPCI Interface

The SCP/DCP-124P cPCI interface is compliant with PICMG 2.0 R3.0 cPCI specification with the J2 connector to PICMG 2.3. One of the Discovery III's two PCI interfaces is used to implement the cPCI bus. It provides a 32-bit, 33/66MHz PCI bus with support for +3.3V and +5V VIO. It is capable of acting as only a peripheral.

PMC Site

The functionality of the SCP/DCP-124P SBC can be expanded via its PCI Mezzanine Card (PMC) site which is compliant to PICMG2.3. The PMC site interfaces to other system elements via up to 64-pins of back panel I/O.

The PMC site is served by an independent 64-bit, 100MHz-capable PCI-X bus off of the Discovery III providing a peak bandwidth to memory of 800MB/s. The PMC bus is shared with the USB device. High-performance PMC modules such as networking modules or graphics modules can operate at 100MHz independent of the speed of the cPCI bus. If the USB device is enabled, the bus is limited to 33MHz PCI.

The SCP/DCP-124P conforms fully to the IEEE 1386/1386.1 requirement for a component keep-out area at the front of the PMC site for connectors or high components.

The PMC site uses 3.3V signaling, is 5V tolerant, and is keyed as a universal PMC site meaning that no keys are installed. The VIO voltage to the PMC is selectable via push-on jumpers.

Routing for High-speed PMC I/O Signals

The SCP/DCP-124P's routing for PMC I/O signals to the rear-panel connectors is carefully implemented to support high-bandwidth signals and is compliant to PICMG 2.3 pin out. The PMC site has the following routing provisions:

- All signals are routed as single-ended 50 Ohm signals with constrain skew between signals of 0.xxxx"
- Pair-to-pair skew is controlled within various pair groupings as required to support multiple TMDS and LVDS digital video channels as implemented on Curtiss-Wright's PMC-70x graphics modules
- Select pairs constrain in-pair skew to 0.012" (nominal) to support two Fibre Channel interfaces as implemented on Curtiss-Wright's fiber channel modules.

Contact your Curtiss-Wright representative for further information on the routing provisions for high-speed PMC I/O.

PMC Power Routing

The PMC site is provided with +5V, 3.3V, +12V, and -12V power from the backplane.

Support for Processor PMCs

The SCP/DCP-124P is capable of hosting processor PMCs in non-Monarch mode as described in the VITA 32-2003 draft standard (the Monarch# signal is left floating). The SCP/DCP-124P does not support the optional second PCI agent, the optional EREADY signal, or the optional RESETOUT# signal.

Conduction-cooled PMC Modules

To support the industry drive to open standards on conduction-cooled cards, the PMC site mechanical interfaces follow the VITA 20- 2001 conduction-cooled PMC standard. To optimize the thermal transfer from PMC modules to the basecard the standard SCP/DCP-124P thermal frame incorporates both the primary and secondary thermal interfaces as defined by VITA 20-2001.

The combination of the secondary thermal interfaces, the mid-plane thermal shunt, and Curtiss-Wright's TherMax Thermal Frame design provides optimum cooling for conduction-cooled PMC modules, allowing for higher power PMCs and/or increased long-term reliability through lower component temperatures.



Status Indicators and Controls

The SCP/DCP-124P SBC provides run/fail status by illuminating a red front panel LED in the event the diagnostics detect a card failure. There is also a software controlled green LED that the application can use to indicate status.

COP, JTAG Test & Debug Interfaces

For software debug purposes the Control and Observation Port (COP) of the MPC7448 processor is accessible via a permanently-installed test connector. The test connector is accessible on all build grades of the SCP/DCP-124P including conduction-cooled. An interface cable is available to provide a standard 2x8 .1" pitch header for JTAG emulators.

To support acceptance testing the SCP/DCP-124P provides a JTAG scan chain accessible on a permanently-installed test connector. The JTAG test chain coverage includes the processor, Discovery III system controller, VMEbus interface chip, core functions FPGA, and USB device. PMC modules are automatically added to the JTAG chain when present.

Temperature Sensors

The SCP/DCP-124P provides a Maxim 6634 located near the card edge and a Maxim 1617 temperature sensor located near the processor. Software can read the temperature sensors at any time through their I2C interface connected via the Discovery III system controller, or receive an interrupt from the sensors when a software programmable over- or under- temperature condition occurs. The 1617 also provides the ability to read the processor die temperature. The temperature sensors are accurate to +/-2.5°C from -40°C to +125°C.

Software Support Foundation Firmware & BIT

The SCP/DCP-124P SBC is equipped with a comprehensive on-board firmware package called Foundation Firmware that includes:

- General Purpose Monitor (GPM) - provides monitoring, diagnostic, and board exerciser functions to facilitate system startup and integration activities
- Built-in-Test (BIT) - a library of Card Level Diagnostic (CLD) routines is provided to support Power-up BIT (PBIT). Initiated BIT (IBIT) and Continuous (CBIT) is also supported for VxWorks.
- Non-Volatile Memory Programmer (NVMP) - provides for in-circuit and closed chassis reprogramming of Flash memory over serial or Ethernet link
- Warm boot/cold boot determination
- SecureErase function to erase all non-volatile memories
- Curtiss-Wright's CLD is designed to provide 95% fault coverage for testable functionality and supports tests in Power-up BIT (PBIT), Initiated BIT (IBIT), and Continuous BIT (CBIT) modes. PBIT consists of a reduced set of tests that provide confidence that the hardware is operating correctly while minimizing power-up time.

The IBIT capability allows users to initiate testing with a more comprehensive suite of tests to provide more robust testing in an off-line mode. CBIT allows applications to test hardware components in the background while the mission software operates as a higher priority task. The selection of tests for PBIT, IBIT, and CBIT is user configurable.

Operating System Software

The SCP/DCP-124P is supported by the following real-time operating systems:

Table 4: SCP/DCP-124P Supported Real-time Operating Systems

Tornado 2.2.x	VxWorks 5.5.x	DSW-124-002-CD
Workbench 2.x	VxWorks 6.x	DSW-124-006-CD
Yellow Dog Linux™ v 4.0	Linux 2.6.x	DSW-124-6100-YLD
- DENX Software Engineering's Embedded - Linux Development Kit (ELDK) 4.0	Linux 2.6.x	DSW-124-6100-ELDK
Wind River Linux GPP LE	Linux 2.6.x	DSW-124-6100-GPP
Green Hill MULTI 4.2.1	INTEGRITY 5.0.7	DSW-124-405-CD

Refer to the separate VxWorks and Linux BSP and Driver Suite datasheet for details.

Contact your Curtiss-Wright representative for updates on support for other operating systems.

Table 5: Cable Set/Development Support

Number	Connects To	Description
CBL-124P-003	J2	Rear panel cable set for SCP/DCP-124P-0x03 mode. The cable provides one 9-pin D connectors for RS-232 port, two 25-pin D connectors for RS-422/485 ports, one 25-pin D connector for DIO, two standard RJ-45 10/100/1000Base-T Ethernet jack, one USB type A receptacle and one push-button switch for card reset. Products supports: SCP-124P-0x03.
CBL-124P-004	J2	Rear panel cable set for SCP/DCP-124P-0x04 mode. The cable provides one 9-pin D connectors for RS-232 port, two 25-pin D connectors for RS-422/485 ports, one 25-pin D connector for DIO, two standard RJ-45 10/100Base-T Ethernet jack, one USB type A receptacle and one push-button switch for card reset. Products supports: SCP-124P-0x04.

Continuum Vector Library

Curtiss-Wright's Continuum Vector DSP library allows customers to fully exploit the performance potential of the Foundation Firmware 124P's AltiVec-equipped MPC7448 processors. Continuum Vector provides a comprehensive set of AltiVec-optimized C-callable functions written primarily in assembly language, yielding a significant performance advantage over equivalent functions written only in a high-level language. This object-format library integrates easily with standard software development tools and supports real and complex array, vector, and scalar signal processing functions.

Product Documentation

Documentation Delivery on DVD-ROM

A standard DVD-ROM (DPK-TechDoc-DVD) is available which includes documentation for the Foundation Firmware SCP/DCP-124P. Providing many ease of use features, the DVD-ROM serves as a complete technical documentation library for the SCP/DCP-124P. Along with the user documentation, a complete library of Product Release Notes is also included.

Pinout Configurator Utilities

The pin-out configurator is a Microsoft® Windows® application that allows users to generate accurate backplane connector pinout tables based upon the customer's specific SCP/DCP-124P configuration. Using a visual point and click interface, users select which PMC module is installed in the PMC site on their basecard, then click a button to generate the precise pinout information, which can then be viewed on-screen, printed, or exported into a common application such as MS-Word.

Convenient Web Links

The interface of the DVD-ROM provides convenient point-and-click access to additional corporate information, contacts and resources, such as Continuum Support, sales and support contacts. (Please consult the Continuum Support web site (http://csc.cwcembedded.com/) periodically to view or download new or updated releases of user documentation that may become available between DVD-ROM releases.)



Power Inputs & Power Consumption

The SCP/DCP-124P uses +5V, +3.3V. On-board regulators provide all other necessary internal voltages. Backplane +5V, +/-12V, and +3.3V is routed to the PMC site.

Power Consumption

See Table 6 for power consumption figures for the SCP/DCP-124P. Power consumption increases as operating temperature rises. Table 6 figures are for the highest rated operating temperature while executing a test application generating CPU processing loads and data traffic representative of a typical customer application.

Table 6: SCP/DCP-124P Power Consumption

Ruggedization Level	Reference Configuration	Max (W)
L000 Air-cooled	SCP-124P-01xx	16
L000 Air-cooled	SCP-124P-04xx	17
L100 Air-cooled	SCP-124P-11xx	19.2
L100 Air-cooled	SCP-124P-14xx	22.1
L200 Conduction-cooled	DCP-124P-21xx	19.2
L200 Conduction-cooled	DCP-124P-24xx	22.1

Notes
1. Typical power figures are measured values.
2. Typical power is measured power while running stress test software that exercises CPU and board functions. AltiVec is not running. The actual power consumption observed will vary by application.
3. For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption figures. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption figures.

Table 7: SCP/DCP-124P Power Supply Specifications

Power Requirements	Typical (A)	Comments
+5V (+5.0%, -2.5%) MPC7448 variant	3.85	See note 1
+12V	0.0	See note 2
+12V	0.0	See note 2
+3.3V	0.9	See note 1

Notes
1. Basecard only. Also routed to the PMC site.
2. Not used by the basecard, only routed to the PMC sites.
3. For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption figures. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption figures.

Mechanical Format

Conduction-cooled modules conform to the dimensions defined in VITA 30.1-2002, American National Standard for 2mm Connector Equipment Practice on conduction-cooled Euroboards.

Air-cooled modules conform to the dimensions defined in ANSI/VITA 1-1994, American National Standard for VME64. Front panel hardware on air-cooled modules includes: injector/extractor handles, alignment pin, and keying provisions in accordance with ANSI/VITA 1.1, American National Standards for VME64 Extensions (and IEEE 1101.10).

Table 8: Dimensions & Weight

Card	Dimensions	Weight (grams)
SCP card	per ANSI/VITA 1-1994	255 (see note 1)
DCP card	per IEEE 1101.2 (see note 2)	335 MPC7448 (see note 1) (includes wedgelocks)

Notes
1. All weight are typical measured values.
2. Except for the card-edge profile as shown in Figure 4

Ruggedization Levels

SCP card — Available in levels 0, 100 (Required airflow is 10 cfm at sea level)
DCP card — Available in levels 100 and 200

Unless otherwise noted environmental tolerance is as defined in Curtiss-Wright's Ruggedization Guidelines factsheet.

Level 100 conduction-cooled is only available by customer specific request.

Part Numbers
Check with Curtiss-Wright representative for availability of specific part numbers.

Note: Please contact your appropriate sales representative for 1GB memory variants.



Part Numbers

Check with Curtiss-Wright representative for availability of specific part numbers.

SCP/DCP - 124P - xyzz

Pin-out mode:
- 3: PICMG 2.3 with GbE, Async RS422
- 4: PICMG 2.3 with 10/100BT, with Sync RS422

Processing core/ Variant:
- 1: MPC7448 @ 1.0GHz, 512MB SDRAM, 256MB Flash
- 4: MPC7448 @ 1.2GHz, 512MB SDRAM, 256MB Flash
- 8: Custom variant

Ruggedization level:
- 0: 0 to 50°C
- 1: -40 to 71°C
- 2: -40 to 85°C

Model number:
- 124P

Cooling method:
- SCP - Convection
- DCP - Conduction

Note: Please contact your appropriate sales representative for 1GB memory variants.

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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