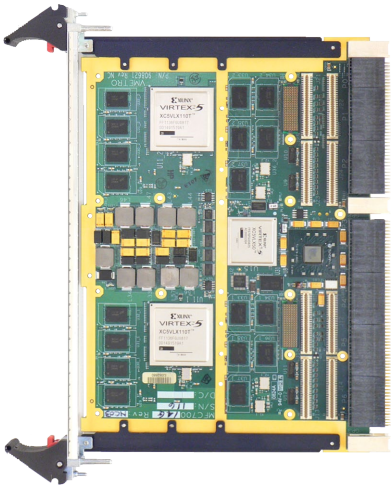
Data Sheet

MFC700

6U VPX-REDI 32GB Memory FPGA XMC Carrier with Serial RapidIO®



Applications

- Image Processing
- Data Buffering
- Snapshot Recording
- Radar

Features

- Up to 32 GB DDR2 SDRAM with ECC
- Four x4 high-speed Serial RapidIO® (sRIO) links to the P1 VPX connector and low-speed I/Os to the backplane
- Onboard 8-port sRIO switch
- Dual Xilinx® Virtex®-5 LX110T FPGA memory controllers
- Additional RocketIO™ connections between FPGAs and the backplane
- Air and conduction-cooled options, 1" pitch
- OpenVPX profile MOD6-PER-4F-12.3.1-n

Overview

The MFC700 is a 6U OpenVPX compatible memory carrier with support for 16 GB of memory on the baseboard, dual XMC mezzanine sites and a Serial RapidIO® (sRIO) fabric. Designed for applications that buffer large amount of high-speed data, the card can be utilized in signal and image processing applications, as well as snapshot and recording subsystems. The dual XMC mezzanine sites provide flexibility for system expansion, specifically for adding additional memory XMCs boosting the total memory capacity to 32 GB. With support for sRIO, the board can complement other Curtiss-Wright Controls Embedded Computing products such as the CHAMP-AV6/AV8, VPX6-185/187, HPE720, and VPX6-472.

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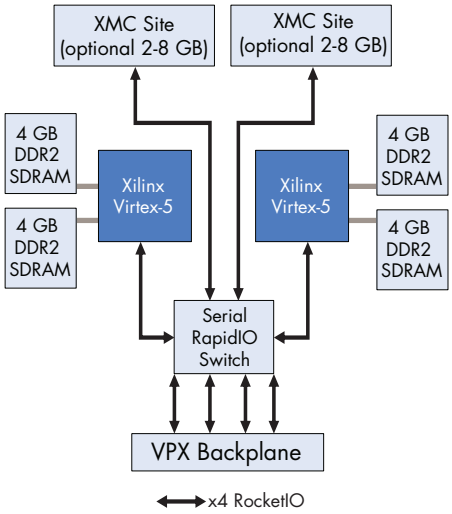
Figure 1: High-level MFC700 Block Diagram

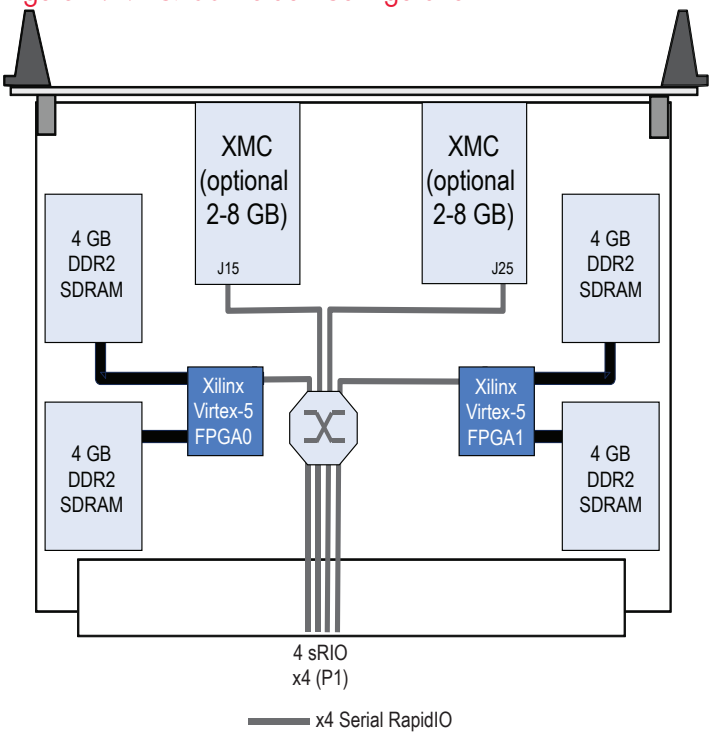


The MFC700 is a large buffer memory board. Buffer memory sits as an endpoint on a fabric or bus, making it accessible to other resources such as FPGAs and processors. Uses of buffer memory include high-speed temporary storage, interleaving, data aggregation and warehousing, or providing additional system memory through a fabric. Buffer memory can act as a target or a master using a DMA engine.

Xilinx® Virtex®-5 FPGA Nodes

The FPGA nodes on the MFC700 combine large memory resources with a variety of I/Os for system needs. The FPGA nodes used on the board are Xilinx Virtex-5 FF1136 package FPGAs. The LX110T device is the default option for the board.

Figure 2: MFC700 Default Configuration

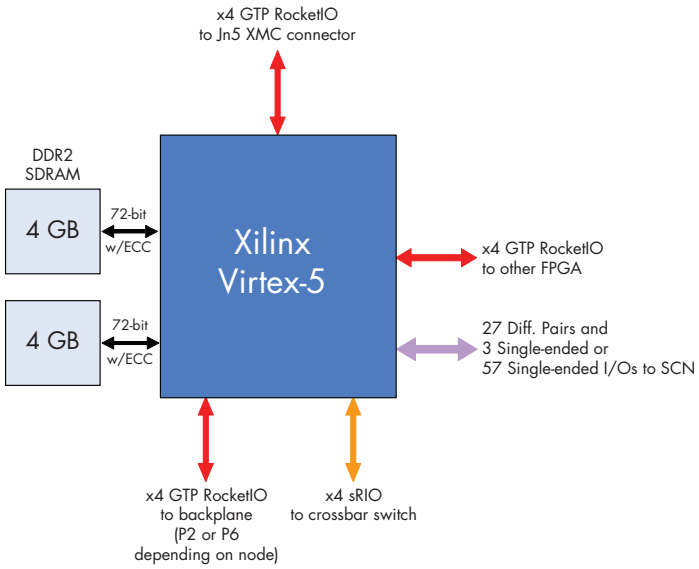


Memory

The FPGA's primary function is as a memory controller. Two large DDR2 SDRAM memory banks connect to each FPGA. Each bank is 72-bits wide with 64-bits for data and 8-bits for ECC. The standard configuration provides 8 GB per FPGA node. These banks run at 200 MHz, providing ample bandwidth for interconnects such as sRIO. Data can simultaneously be placed in one bank while DMA'd out of the other. This allows applications to take advantage of the full-duplex property of sRIO. By default, the board is supplied with a memory controller bit-stream that supports sRIO and does not support User Programmable Logic (UPL). Please contact the factory for applications that require user programming of the FPGA.

16 MB of flash for each FPGA node is available for storing bit-streams.

Figure 3: FPGA Memory and I/O Diagram



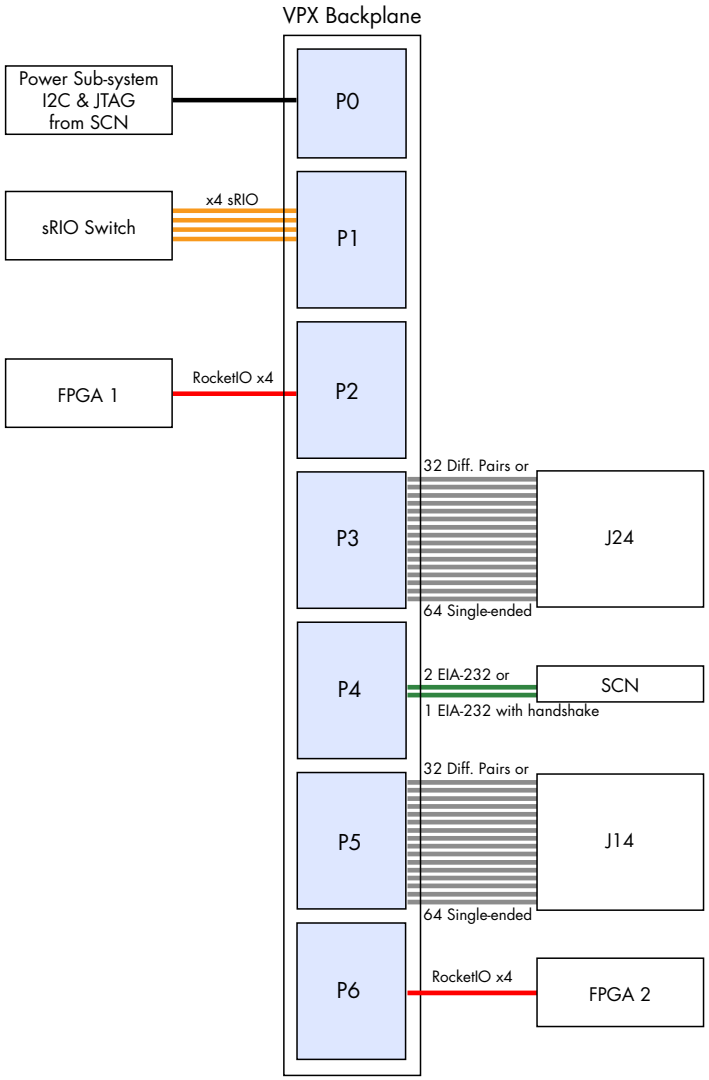
FPGA I/O

The FPGA nodes provide access to the sRIO fabric, RocketIO and low-speed I/O to satisfy a variety of applications. The FPGAs use a 3.125 GB/s x4 link to connect to the sRIO switch. The FPGAs also include an advanced, corner-turning DMA engine, which is especially useful in matrix transposition, where converting from columns to rows can eliminate significant processor overhead. The sRIO switch links can be connected to other sRIO switches and endpoints, allowing the memory resources from the FPGA to be visible to all other parts of the system. The links support full-duplex transfers, enabling ping-pong transactions to the memory controllers or other I/Os of the device.

I/O capabilities for the FPGA nodes include RocketIO connections to the backplane, XMCs and between the FPGAs. A x4 link connects each FPGA to the backplane, using the P2 and P6 connectors. The RocketIOs can be used for protocols such as Aurora™, Serial FPDP (sFPDP) or other high-speed serial interconnects. RocketIO links between the FPGAs provide a low-overhead, high-speed connections where the FPGAs can compare data or do a transfer without going through sRIO.

Backplane I/O

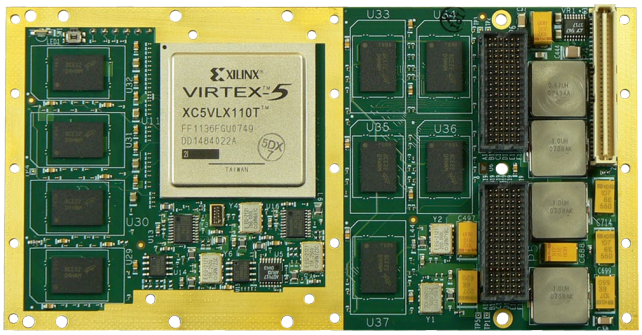
Figure 4: Backplane connectivity



Mezzanine Sites

The MFC700 includes two XMC (VITA 42) mezzanine sites. Each site can connect to the sRIO switch. This gives users the capability to access the sRIO fabric, specifically with the Curtiss-Wright MM-6171 Buffer Memory XMC module with up to 8 GB of memory. The MFC700 with two MM-6171s provides up to 32 GB of memory per slot (16 GB on the MFC700 baseboard and 8 GB per mezzanine site).

Figure 5: MM-6171 2-8 GB Buffer Memory XMC with sRIO



The mezzanines are also equipped with a Jn4 PMC connector, which can route up to 32 differential pairs or 64 single-ended I/Os to the backplane. These signals are routed from one mezzanine to the P3 VPX connector and the other to the P5 VPX connector.

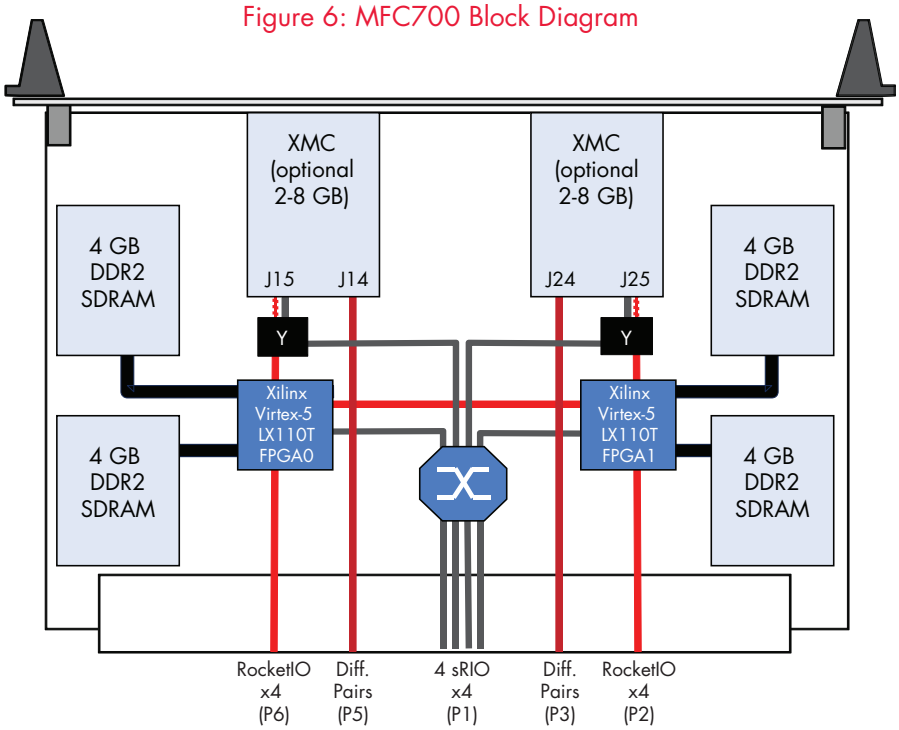
Software

The MFC700 supports Wind River® VxWorks® 6.5 and Wind River® GPP Linux® 2.6.x. An API is provided for integration with other boards.

Ruggedization Levels

The MFC700 is supported with software drivers that run on SRIO-based VPX processor cards. VxWorks 6.x and Linux are supported. The MFC700 software is designed to also integrate with systems running the Curtiss Wright Inter-Processor Communications Library (IPC).

Figure 6: MFC700 Block Diagram



Serial RapidIO x4
HSS (RocketIO) x4, 3.125 Gbps
Differential Pairs & Single-ended I/C
Optional HSS (RocketIO) x4, 3.125
Y I/O Switch



Table 1: Specifications

Memory	
Sizes (Sum of all four banks)	16 GB
Expansion Memory (via XMC sites)	2-8 GB per site when using MM-6171 Buffer Memory XMCs
Bus Width per Array	72-bits wide (64-bit data and 8-bit ECC)
Memory Array Speed	200 MHz
FPGA	
Device	Xilinx Virtex-5 LX110T (consult factory for others)
No. of FPGAs	2
Connectivity	◆ x4 sRIO to each XMC connector ◆ x4 sRIO to switch ◆ x4 GTP RocketIO to backplane (P2 & P6) ◆ x4 GTP RocketIO between FPGAs
Configuration	JTAG, off-board I/Os and onboard flash
Mezzanine Sites	
No. of Sites	2
XMC VITA 42	Jn5 – supports sRIO x4 to switch by default
VPX VITA 46.9	Jn4 – supports 64 single-ended signals or 32 differential pairs to P3 and P5
Serial RapidIO	
Switch Device	Tundra Tsi578 8-port switch
Connectivity	Both FPGAs, both XMCs, 4 connections to P1 fabric connector, all lanes at 3.125 GB/s
Serial I/O	EIA-232 with handshake or 2 EIA-232s from SCN to P2
Backplane	
Compliance	VPX (VITA 46) and VPX REDI (VITA 48)
Connectivity	◆ Power and SCN utility signals (I2C) ◆ 4 sRIO x4s to switch ◆ RocketIO x4 from FPGA 1 ◆ 32 differential pairs or 64 single-ended I/Os from J24 ◆ 1 EIA-232 with handshake or 2 EIA-232s from SCN ◆ 16 differential pairs or 32 single-ended I/Os from SCN ◆ 32 differential pairs or 64 single-ended I/Os from J14 ◆ 1 x4 RocketIO link from FPGA 0 ◆ 16 differential pairs with 2 single-ended I/Os or 34 single-ended I/Os from SCN

Software	
Operating System	Wind River VxWorks 6.x, Wind River Llnux
Standards	
Compliance	VITA 20, 42.0, 42.2, 42.3, 46.0, 46.3, 46.9 and IEEE 1386
Miscellaneous	
Power	VPX ◆ 5 V ◆ +12 V
Cabling	JTAG cable and adapter (p/n JTAG-1001)
Weight	◆ Air-cooled: 2.6 lbs (1.18 kg) ◆ Conduction-cooled: 3.21 lbs (1.45 kg)

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

Technical Support

For technical support:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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