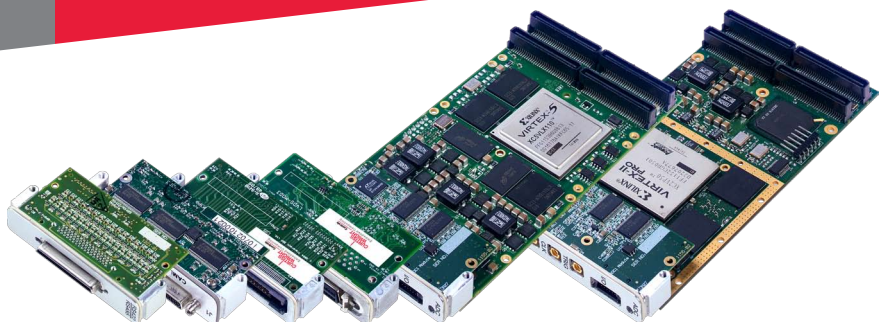
Data Sheet

I/O Modules for FPGA Processors

Analog Input/Output, Camera Link, LVDS & RS-422/485



Applications

- RADAR/LIDAR
- Electronic Warfare
- Signal Intelligence (SIGINT)
- Surveillance
- Real-time imaging / Inspection / Machine vision
- Medical Imaging
- Satellite Modems

Choice of I/O Modules

- Dual Channel, 125MSPS Analog Input
- Dual Channel, 210MSPS Analog Output
- Camera Link
- LVDS
- High Density LVDS
- 33 Channel RS485/422

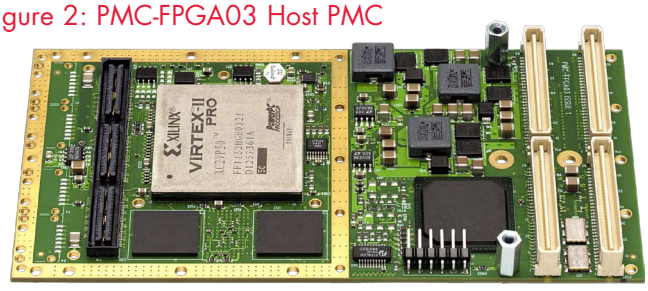
Overview

A range of I/O modules are available for use with Curtiss-Wright's Xilinx® Virtex-II Pro based PMC-FPGA03 and the Xilinx® Virtex®-5 based PMC-FPGA05 and XMC-FPGA05D products. These modules allow the host FPGA PMC/XMC to have a choice of I/O connected directly to the FPGA. This removes bottlenecks and provides a highly integrated processing solution with I/O.

FPGA Accelerated I/O

Figure 1: PMC-FPGA05 Host PMC

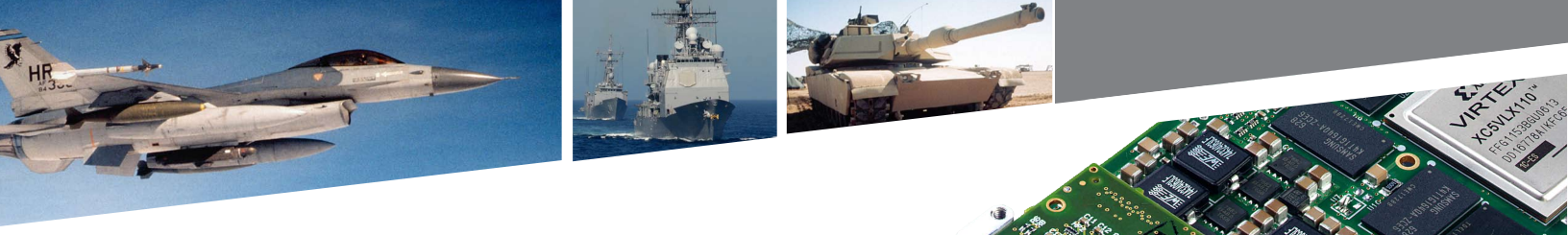
Figure 2: PMC-FPGA03 Host PMC



Learn More
Web / sales.cwcembedded.com
Email / sales@cwcembedded.com

CURTISS WRIGHT Controls
Embedded Computing

Innovation In Motion.
cwcembedded.com



Custom I/O Modules

Conceptually, the I/O modules for PMC-FPGA03, PMC-FPGA05 and XMC-FPGA05D products are simple: the module includes just analog converters or transceivers, buffers and connectors. The host FPGA controls the interface timing and data handling. The simplicity of the modules means that new application specific modules are straightforward to develop (provided that there is sufficient PCB space). A design reference is available for developing new modules.

Connectivity

The module host connector provides up to 138 signals directly connected to the FPGA. These are routed as LVDS pairs to maximize both the flexibility and data speed. The FPGA is programmed to determine the interface characteristics such as impedance. Four of the digital I/O pairs can be local or global clock signals depending on the host board's capabilities.

The host module connector also provides a number of power supplies (2V5, 3V3 and 5V). This minimizes the space required for module specific power supply generation leaving more resource (PCB space) for the module's I/O.

Figure 3: Generic I/O Module Connectivity

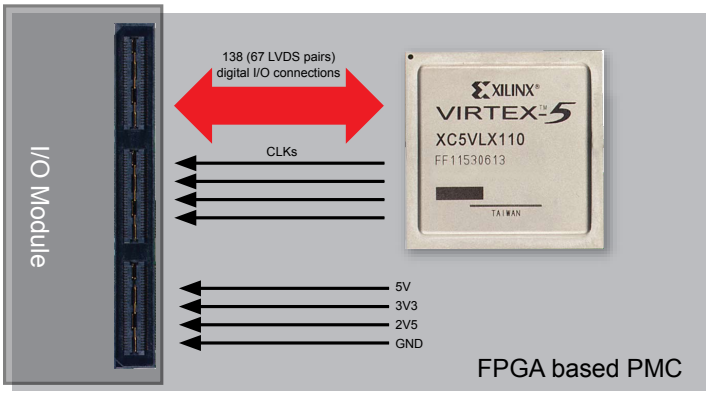


Figure 4: Modules fitted to Virtex-5 PMCs (above)
Virtex-II Pro PMCs (below)

Dual 125MSPS Analog Input Module (ADC-MOD2)

The ADC-MOD2 is a general purpose dual channel 14-bit analog input module. The ADC-MOD2 has an on-board 125MHz oscillator as well as provision for an external clock source. The sampling clock and trigger are made available to the host FPGA for complete application control. General purpose digital I/O signals are routed through to the front panel and are also controlled by the host FPGA. These can be used for synchronizing multiple boards or alternative trigger mechanisms. Applications include Software Defined Radio, radar and telecommunications.

Figure 5: ADC-MOD2 Block Diagram

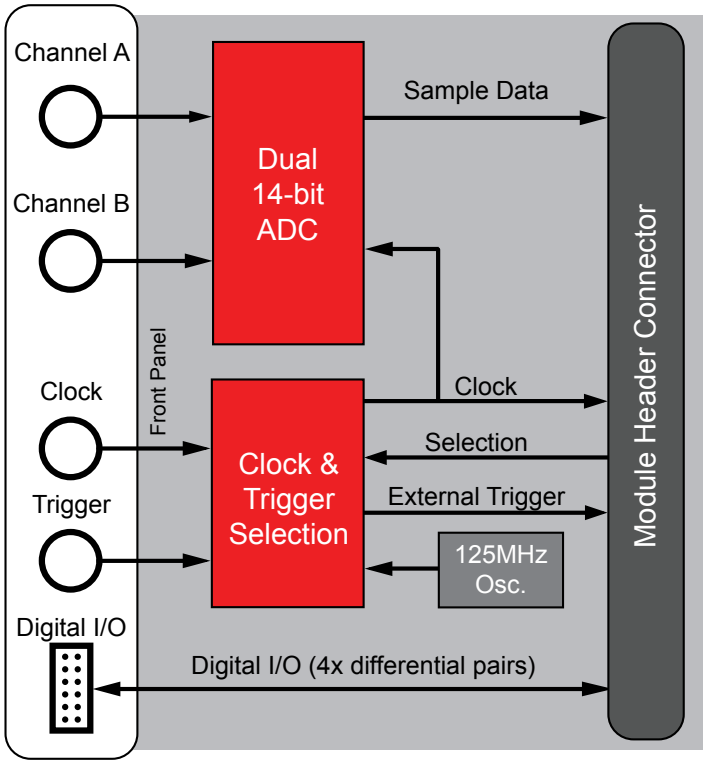


Table 1: ADC-MOD2 Specifications

Analog Inputs	
Number of Channels	2, single-ended
ADC Device	LTC2285
Device Resolution	14-bit
Sampling Frequency	1 to 125MHz
Full Scale Input Voltage	2 Vpk-pk (+10dBm) contact Curtiss-Wright for alternative input ranges
Full Power Input Bandwidth	100kHz to 110MHz
Input Impedance	50Ohm, AC coupled
SNR (at 10MHz)	68dB
SFDR (at 10MHz)	82dB
Clock & Trigger Inputs	
External	Front panel MMCX
Input Frequency Range	1 to 125MHz
Input level	200-1000mVpk-pk (sine or squarewave)
Input impedance	50Ohm, AC coupled LVPECL
Trigger	Single-ended, 50Ohm, DC coupled
Clock Selection	Controlled by FPGA
Digital I/O	
Number	4x differential pairs
Connector	12-way IDC

Dual 210MSPS Analog Output Module (DAC-MOD1)

The DAC-MOD1 is a dual channel 14-bit analog output module with an on-board 210MHz oscillator and provision for external clock sources. The sampling clock and trigger are made available to the host FPGA for application control. Digital I/O signals are routed to the front panel and are controlled by the host FPGA. These can be used for synchronizing multiple boards or as an alternative triggers.

Figure 6: DAC-MOD1 Block Diagram

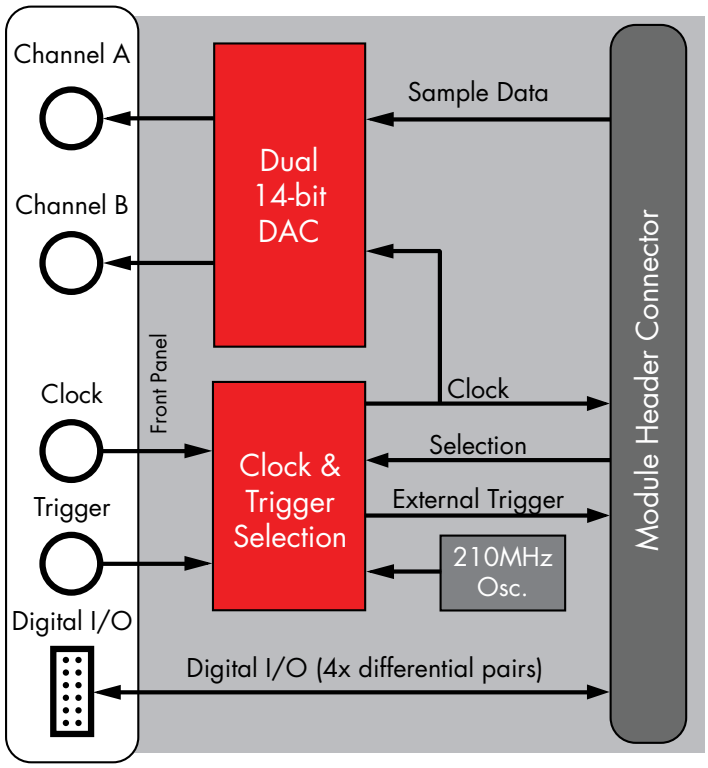


Table 2: DAC-MOD1 Specifications

Analog Outputs	
Number of Channels	2, single-ended
DAC Device	Analog Devices 9744
Device Resolution	14-bit
Sampling Frequency	210MHz
Full Scale output Voltage	0.5Vpk-pk
Output Bandwidth	300MHz
Output Impedance	50Ohm, AC coupled (contact Curtiss-Wright for DC coupled variant)
Connectors	Front panel MMCX
Clock & Trigger Inputs	
External	Front panel MMCX
Input level	1Vpk-pk (sine or squarewave)
Input impedance	50Ohm, AC coupled LVPECL
Trigger	Single-ended, 50Ohm, DC coupled, LVPECL
Internal Clock	Low jitter 210MHz Oscillator
Clock Selection	Controlled by FPGA
Digital I/O	
Number	4x differential pairs
Connector	12-way IDC



Camera Link Module

(CAML-MOD3)

The Camera Link module provides either two [base] camera inputs or one [medium/full] camera input. Base mode provides 8-bit input; medium and full provide 16- and 24-bits respectively. 24-bit is suitable for RGB cameras (R: 8-bit, G: 8-bit and B: 8-bit). Ideal applications include inspection systems and medical imaging.

Figure 7: CAML-MOD3 Block Diagram

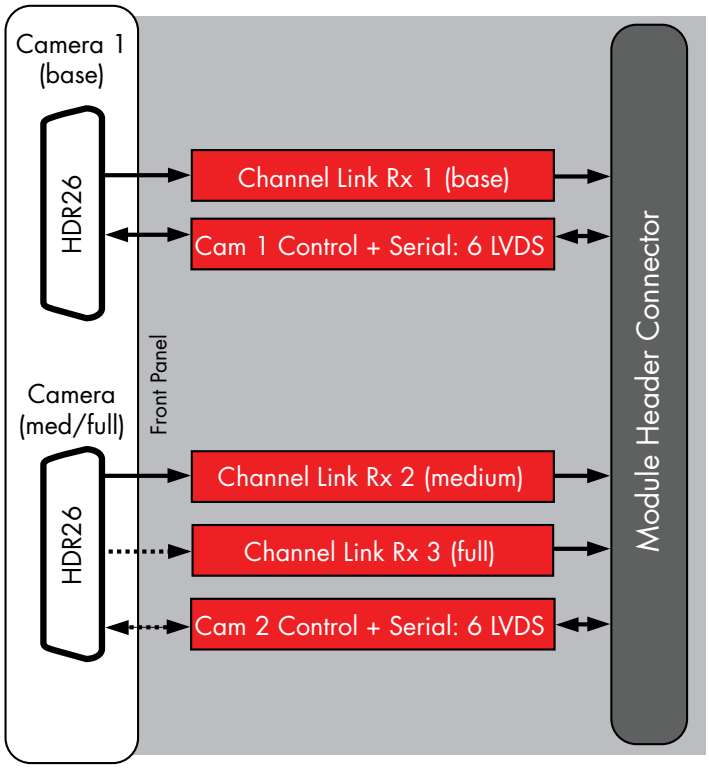
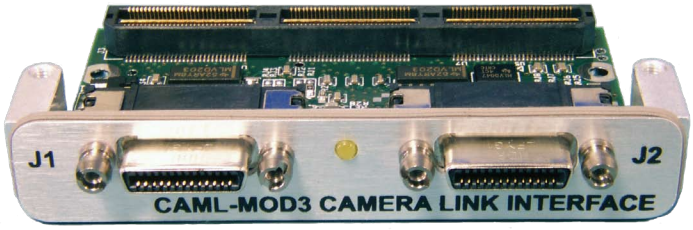


Table 3: CAML-MOD3 Specifications

Camera Link Inputs	
Front Panel J1	Base camera
Front Panel J2	Medium/Full extension, or 2nd Base camera
Connector type	Mini Camera link, Honda HDR-EA26LFYPG1- SLG
Channel Link Receiver	National Semiconductor DS90CR288A
Maximum Bandwidth (at 85MHz Camera Link clock)	Base mode: 255MB/s, per camera Medium mode: 510MB/s, 1 camera Full mode: 680MB/s, 1 camera
Camera Control & Serial Communication	CC[4..1]: Fully implemented Serial UART: Implemented in FPGA, 9600 to 921600 Baud

Figure 8: Camera Link Interface Module



LVDS Module

(LVDS-MOD3)

The LVDS-MOD3 module is a general purpose I/O module effectively connecting an FPGA directly to the external connector. All impedances, data flow and timing are defined by the host FPGA. The signals are routed to a SCSI-3 connector with a compliant pin-out. This means that off-the-shelf differential SCSI-3 cables can be used which simplifies system development and reduces cost.

Figure 9: LVDS-MOD3 Block Diagram

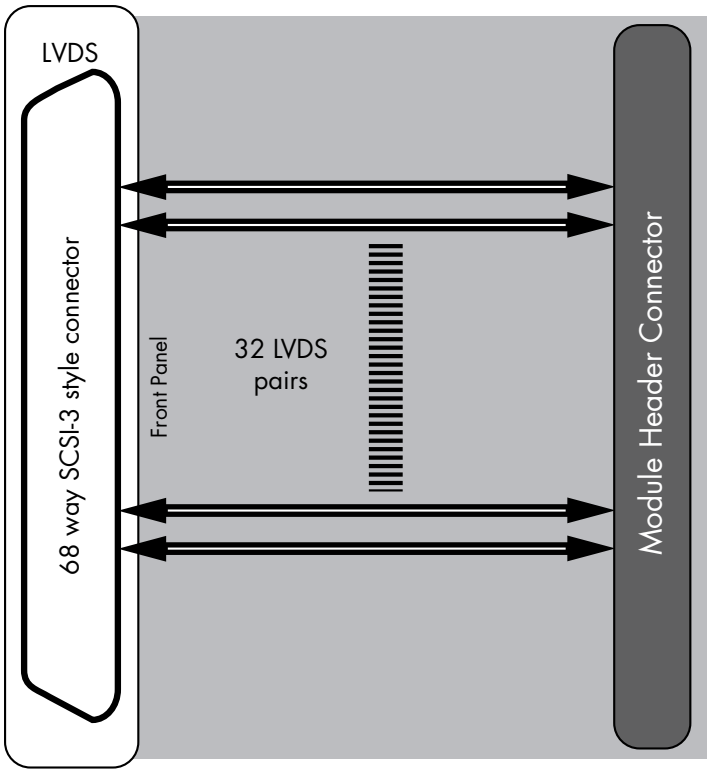
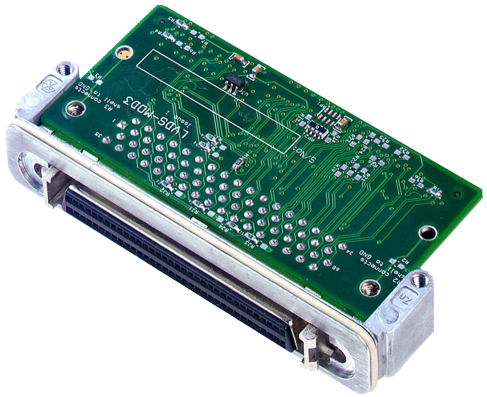


Table 4: LVDS-MOD3 Specifications

LVDS	
LVDS	32 differential pairs
Connector	Front panel SCSI-3 style
Signaling	2.5/3.3V

Figure 10: LVDS-MOD3



High Density LVDS Module (LVDS-MOD4)

The LVDS-MOD4 module is a general purpose I/O module effectively connecting an FPGA directly to the external connector. The LVDS-MOD4 provides 2x as many connections as the LVDS-MOD3; 64 LVDS pairs as opposed to 32 LVDS pairs. All impedances, data flow and timing are defined by the host FPGA. The signals are routed out to a high-density connector with a compliant pin-out.

Figure 11: LVDS-MOD4 Block Diagram

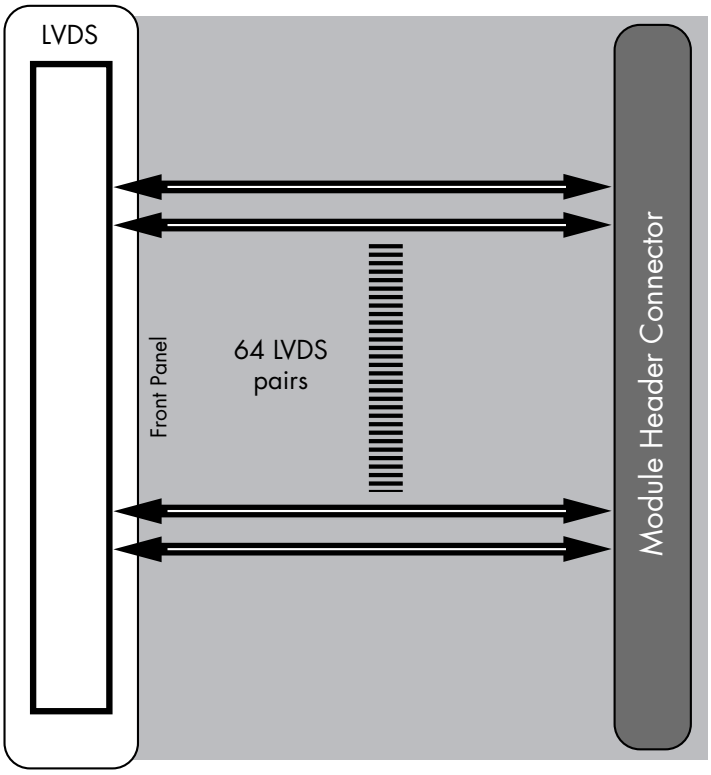
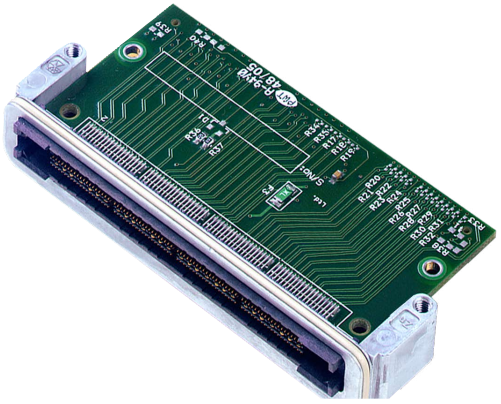


Table 5: LVDS-MOD4 Specifications

High Density LVDS	
LVDS	64 differential pairs
Connector	AMP/Tyco 767044-4
Signaling	2.5/3.3V

Figure 12: LVDS-MOD4





High Density LVDS Module (LVDS-MOD5)

The LVDS-MOD5 is a high density LVDS module which offers the benefits of simplified cable connectivity by using two digital I/O headers suitable for ribbon cables. The LVDS-MOD5 can be used for a mixture of 2.5V and 3.3V input and output signals depending upon the VCCO settings on the FPGA on any particular I/O bank. The LVDS-MOD5 provides two 80 way ERNI IDC front panel connectors, each supporting 26 differential pairs (each pair can be used as two single-ended signals). All impedances, data flow and timing are defined by the host FPGA. The signals are routed out to a high-density connector with a compliant pin-out.

Figure 13: LVDS-MOD5 Block Diagram

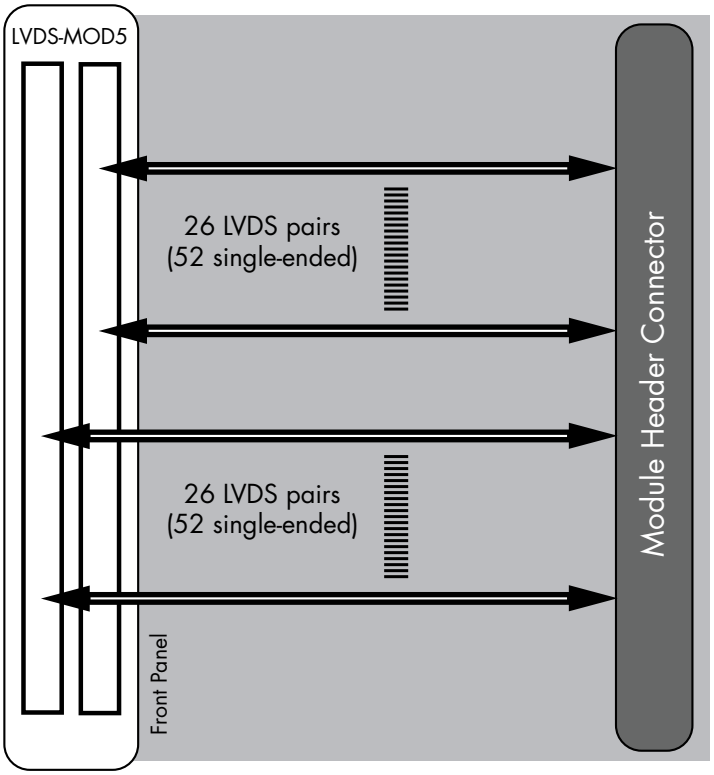


Table 6: LVDS-MOD5 Specifications

High Density LVDS	
LVDS	2x 26 differential pairs
Connector	2x 80 way front panel ERNI 144806
Signaling	2.5/3.3V



RS485/422 Module

(RS485-MOD2)

The RS485-MOD2 provides 33 channels of RS485 I/O; each channel can be configured as an input or output (note some channels are defined in blocks of four). Compliant on-board drivers allow either RS485 or RS422 to be supported. A single 68-way VHDCI (SCSI-5 style) connector provides access to the signal using a pinout that allows standard differential SCSI-5 cables to be used [only SCSI-5 cables where all 34 pairs are made using twisted pair cabling should be used]. This simplifies use and minimizes cost. Serial protocols and timings are handled by the host FPGA.

Figure 14: RS485-MOD2 Block Diagram

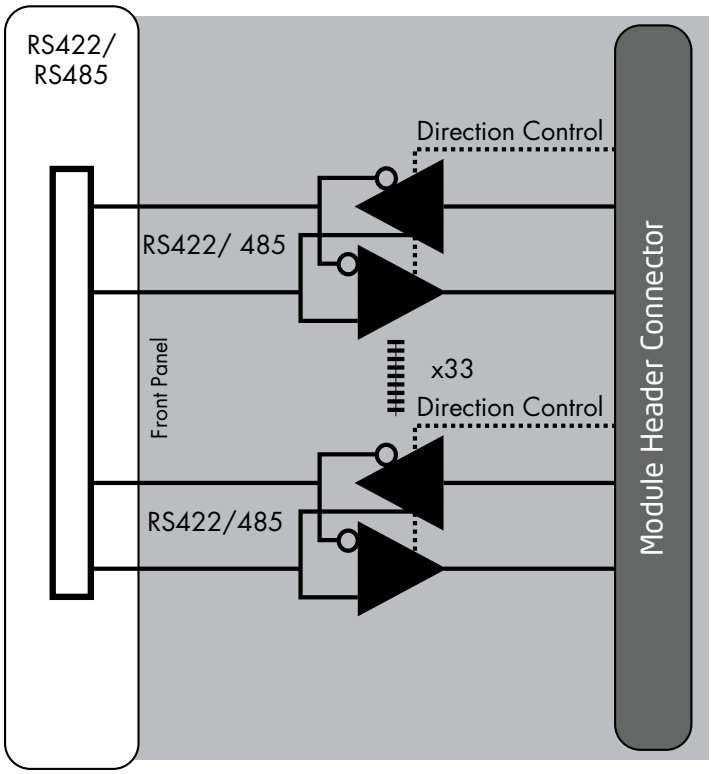


Table 7: RS485-MOD2 Specifications

Serial I/O	
RS422/485	33 pairs (configurable as input or output) + 2 GN
Connector	VHDCI SCSI-5 style
Input Bandwidth	20Mbps per channel

Figure 15: RS485-MOD2

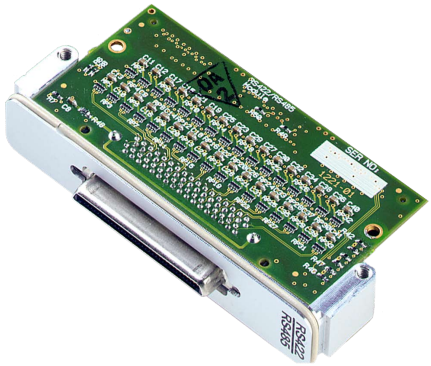




Table 8: Ordering Information

Analog Input/Output	
ADC-MOD2	Dual channel, 125MS/s 14-bit ADC module
DAC-MOD1	Dual channel, 210MS/s 14-bit DAC module
CBL-2MMCX-100	100cm MMCX to MMCX cable
CBL-2MMCX-22	22cm MMCX to MMCX cable
CBL-MMCX-BNC-100	100cm MMCX to BNC cable
LVDS	
LVDS-MOD3	32-LVDS pair I/O module
LVDS-MOD4	64-LVDS pair I/O module
LVDS-MOD5	2x 26 LVDS pair module
Camera Link	
CAML-MOD3	Two base camera inputs (or one medium) I/O module
RS485/RS422	
RS485-MOD2	33x channel RS485/RS422 I/O module
FPGA PMC/XMC Module	
PMC-FPGA03	Please see product specific datasheet
PMC-FPGA05	Please see product specific datasheet
XMC-FPGA05D	Please see product specific datasheet

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

The information in this document is subject to change without notice and should not be construed as a commitment by Curtiss-Wright Controls Embedded Computing. While reasonable precautions have been taken, Curtiss-Wright Controls assumes no responsibility for any errors that may appear in this document. All products shown or mentioned are trademarks or registered trademarks of their respective owners.