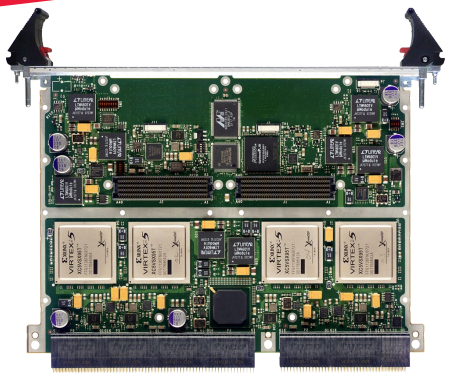
Data Sheet

FPE650

Quad Xilinx® Virtex®-5 6U Processor



Applications

The FPE650 is ideal for digital signal processing (DSP) applications including:

- Signal Intelligence (SIGINT)
- Electronic Counter Measures (ECM)
- Radar

Features

- x4 Xilinx Virtex-5 FPGAs (SX95T)
- Dual FPGA mezzanine card (FMC/VITA 57) sites
- Multiple banks of FPGA connected QDR SRAM and DDR SDRAM memory
- 6U VPX form factor
- Commercial and rugged build options (air- and conduction-cooled)

Benefits

- High-performance processing
- High-bandwidth I/O between front-panel or backplane and the FPGA processors
- Suitable for use in severe environments
- Industry standard form factor

Overview

The FPE650 is a quad FPGA processor card which combines high-performance and high-bandwidth I/O in a flexible format. Provided in a 6U VPX (ANSI VITA 46) format, the FPE650 has a large number of multi-Gigabit/s serial and parallel data links to the backplane as well as FMC (VITA 57) mezzanine sites for direct I/O to the FPGAs without introducing data bottlenecks. Each of the FPGAs include multiple banks of memory to help maximize the capabilities of the Xilinx® SX95T FPGAs.

FPGA Nodes

The FPE650 includes four fully user programmable FPGA nodes and are arranged in two FPGA node pairs; two are associated with front panel mezzanine sites. Apart from connectivity, the main difference between the FPGA node pairs is the memory architecture. The FPGA nodes are built with Xilinx SX95T platforms.

All the FPGAs are inter-connected by high-bandwidth data links formed with a mixture of multi-GB/s (x4 RocketIO™) links and parallel data ports. There are additional links that can be configured through an onboard crossbar switch to tune data flow topology. In addition to the onboard data links, all FPGAs have direct connection to the VPX backplane.

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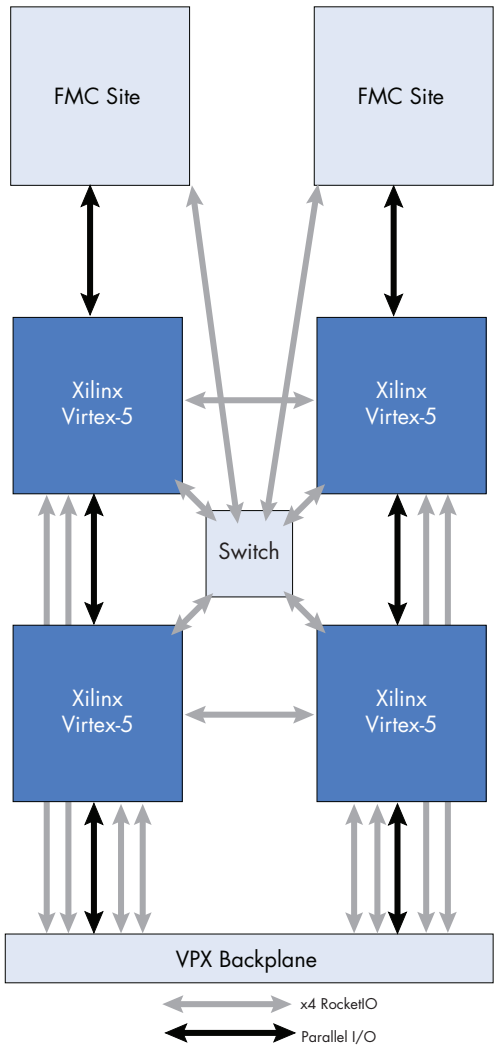
Figure 1: High-level FPE650 FPGA architecture



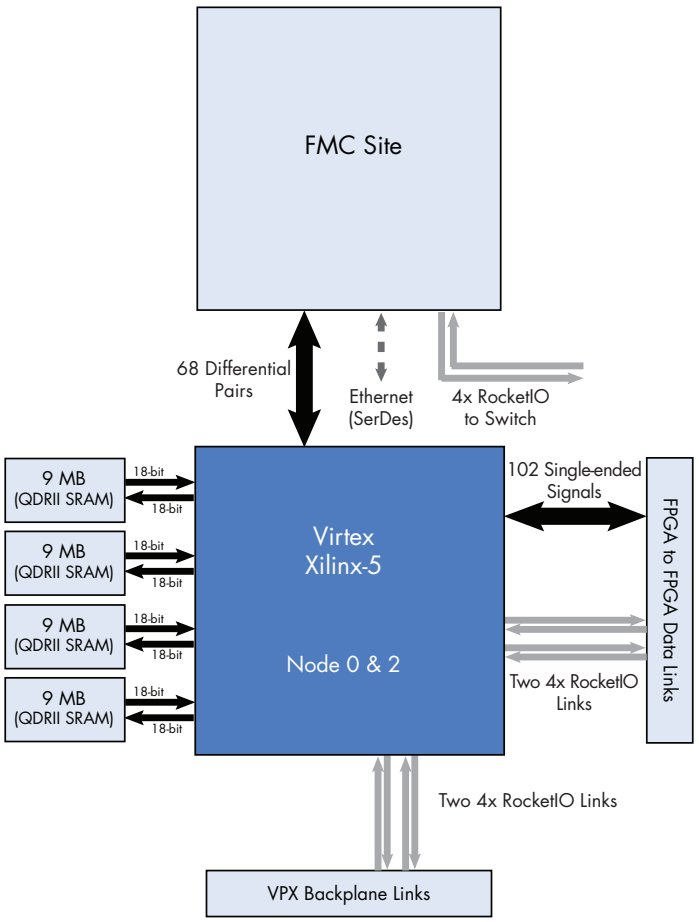
Xilinx Virtex-5 FPGAs

The FPE650 is fitted with Xilinx® Virtex®-5 SXT FPGAs. Please contact Curtiss-Wright Controls Embedded Computing (CWCEC) for the availability of other FPGA variants. The SX95T device is optimized for a high ratio of DSP blocks to standard logic blocks in order to support the high-performance signal processing required by software defined radio, signal intelligence and radar.

FMC FPGA Nodes

Node 0 and node 2, 'FMC FPGA nodes', have their own FMC site providing 68 differential connections and a x4 RocketIO links for high-bandwidth and flexible I/O options. FMC FPGA nodes require high-bandwidth memory to deal with sensor I/O at maximum bandwidth and provided by the FPE650. The FMC FPGA nodes each have four banks of QDRII SRAM (4 M x 18-bit per bank). If more bandwidth is required, these memories can be operated in parallel.

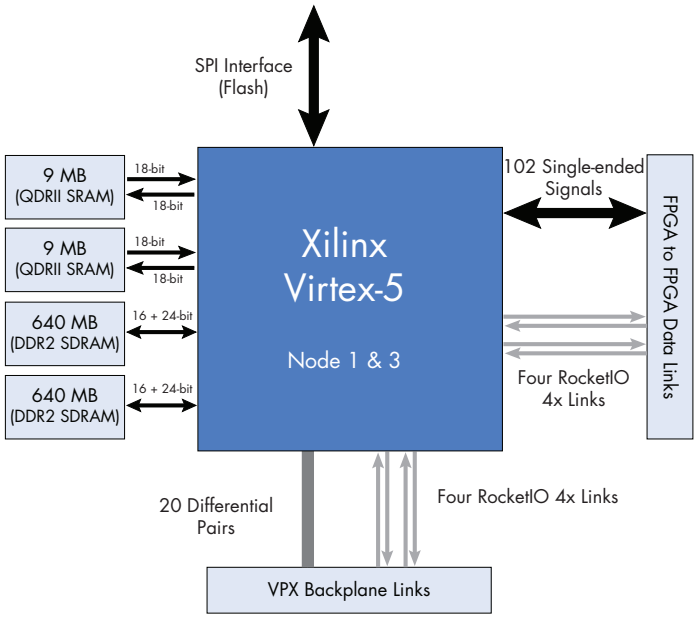
Figure 2: One of two FMC FPGA nodes



Backplane FPGA Nodes

Nodes 1 and 3, 'backplane FPGA nodes', have x4 RocketIO links to the backplane. The FPGAs associated with the backplane have a different memory architecture to those connected to the front panel FMC sites. The backplane nodes' memory has a requirement for higher capacity storage to maintain and buffer system communications. These FPGA nodes have four banks of DDR2 SDRAM structured as a pair of 128 M x 16-bit and 128 M x 24-bit. There also two SRAM banks (4 M x 18-bit each) per FPGA. There is also a user programmable parallel data port per FPGA for flexible backplane based parallel I/O.

Figure 3: One of two backplane FPGA nodes



128 MB of flash memory is provided. This flash is assigned for user applications.

FPGA RocketIO Reference Clocks

The FPE650 has three reference clocks that can be used to determine the GTP clock spread (see GTP speed/clock source table). The protocol is determined through the FPGA configuration choosing the appropriate source and using the FPGA's multiplier and dividers. Currently, direct HDL support is for Aurora.

Table 1: GTP speed/clock sources

Speed	Protocol	Clock Source
3.125 GB/s	SRIO type 3, XAUI, Aurora	125 MHz
2.5 GB/s	SRIO type 2, Aurora, sFPDP	125 MHz
2.5 GB/s	PCIe	100 MHz
2.125 GB/s	2x Fibre Channel, Aurora, sFPDP	106.25 MHz
1.25 GB/s	1x GbE, Aurora	125 MHz
1.0625 GB/s	1x Fibre Channel, Aurora, sFPDP	106.25 MHz
FMC dependent	FMC can supply clock for FPGA	FMC site 1
FMC dependent	FMC can supply clock for FPGA	FMC site 2

FMC Sites

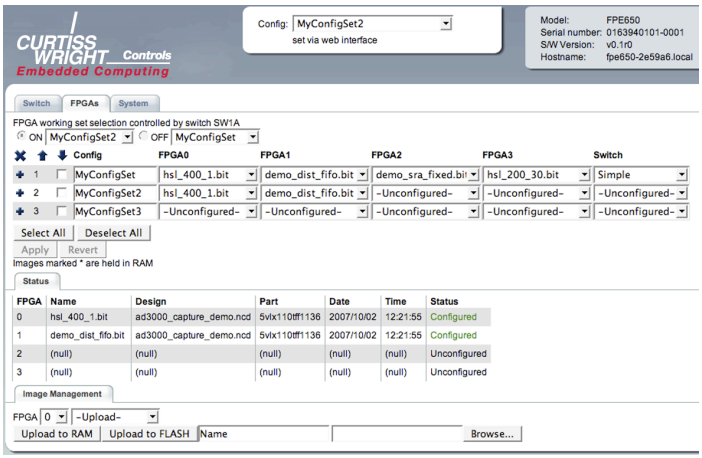
The FPE650 has two FMC sites, each connected to a single FPGA with a parallel 68 differential pair interface. A high-speed x4 serial I/O data link is also routed to each FMC site via the crossbar switch enabling any of the FPGAs or remote off-board device to control and use this interface. The inclusion of FMC sites allows high-bandwidth I/O directly to the FPGAs with little or no data bottlenecks for an efficient I/O to processor solution. FMC bandwidths can support multi-Gbyte/sec data interfaces with minimal latency as the I/O devices on the FMC are directly connected to the FPGA.

Configuration Control & Board Management

FPGA Configuration

The FPE650 includes a Configuration Control Processor (CCP) to manage the configuration images for all of the FPGAs. Images can be uploaded and stored in flash or SDRAM. SDRAM has the added advantage of not retaining data when powered off. This is useful for some secure applications where no trace must be left when the board is not in use. Configuration of the FPGAs can be done automatically on power up or updated as required. 128 MB of flash is provided for FPGA configuration and is large enough to store up to two images per FPGA depending on the type of FPGA platforms fitted.

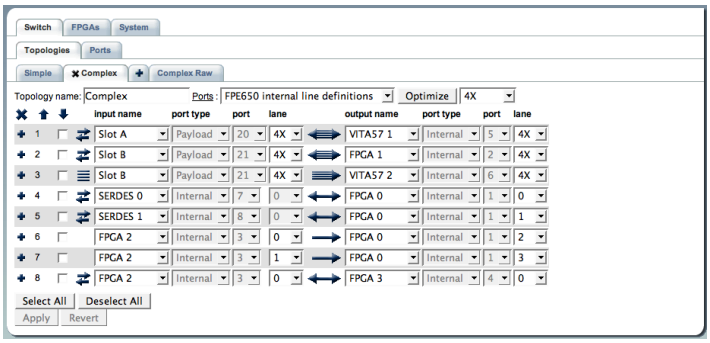
Figure 4: FPGA configuration status accessible through Ethernet/HTML browser interface



Crossbar Switch

Some of the multi-Gbps/RocketIO data link routings onboard the FPE650 can be defined using a crossbar switch. This can be used to direct serial I/O from the FMC to a particular FPGA (including multi-casting modes) or define some inter-FPGA links. The switch is data rate independent and has very low latency. The user interface to control this is via the CCP Ethernet connections using a browser/web server interface for convenience. The crossbar switch is able to support data signaling up to 3.2 GB/s (note: FX100T FPGAs are able to run faster than this, but only to direct backplane connections).

Figure 5: Crossbar switch configuration via Ethernet/HTML browser interface



System Monitoring & Management

The FPE650 has built in temperature and power supply voltage levels sensors across the board and within the FPGAs. This is included within the FPE650 Baseboard Management Controller (BMC) which is common function access CWCEC VPX boards. The BMC also controls critical power supply initialization to safely power the FMC sites and control the VPX adjustable power supplies.

Network Interface

The FPE650 has a user interface that is accessible through any of the FPE650 board's Ethernet ports. This is HTML based for convenience such that any computer running a browser and Ethernet connection can be used without needing any additional applications or utilities. The FPE650 has Ethernet ports available through both the front panel (via the FMC site) or through the backplane. If the front panel FMC based Ethernet port is used, CWCEC can supply a suitable break-out module, the FTM-01.

Figure 6: Ethernet connectivity to the configuration control processor

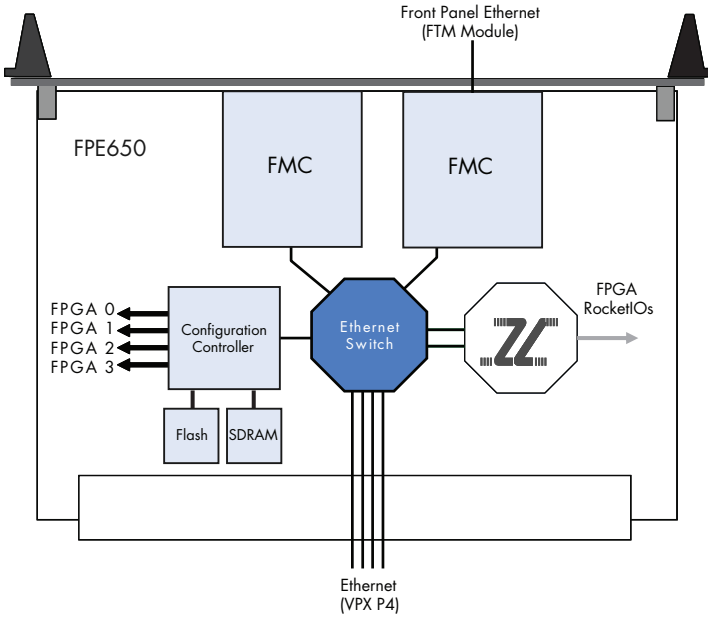


Table 2: VPX backplane connections

VPX Connector	Function	Device
P0 (power)	VS1	+12 V
	VS2	+12 V
	VS3	+5 V
	Auxiliary power supplies	+3 V 3
	System	Various
P1	x4 RocketIO GTP/GTX	FPGA Node 1
	x4 RocketIO GTP/GTX	FPGA Node 1
	x4 RocketIO GTP/GTX	FPGA Node 0
	x4 RocketIO GTP/GTX	FPGA Node 0
P2	x4 RocketIO GTP	Crossbar switch
	x4 RocketIO GTP	Crossbar switch
P3	20 differential pairs	FPGA Node 1
P4	4 Ethernet SerDes ports	Ethernet switch (configuration control processor, both FMC sites and crossbar switch)
	BSYNC	Global clock input to all FPGAs
P5	x4 RocketIO GTP/GTX	FPGA Node 2
	x4 RocketIO GTP/GTX	FPGA Node 2
	x4 RocketIO GTP/GTX	FPGA Node 3
	x4 RocketIO GTP/GTX	FPGA Node 3
P6	20 differential pairs	FPGA Node 3

VPX Serial I/O Communications

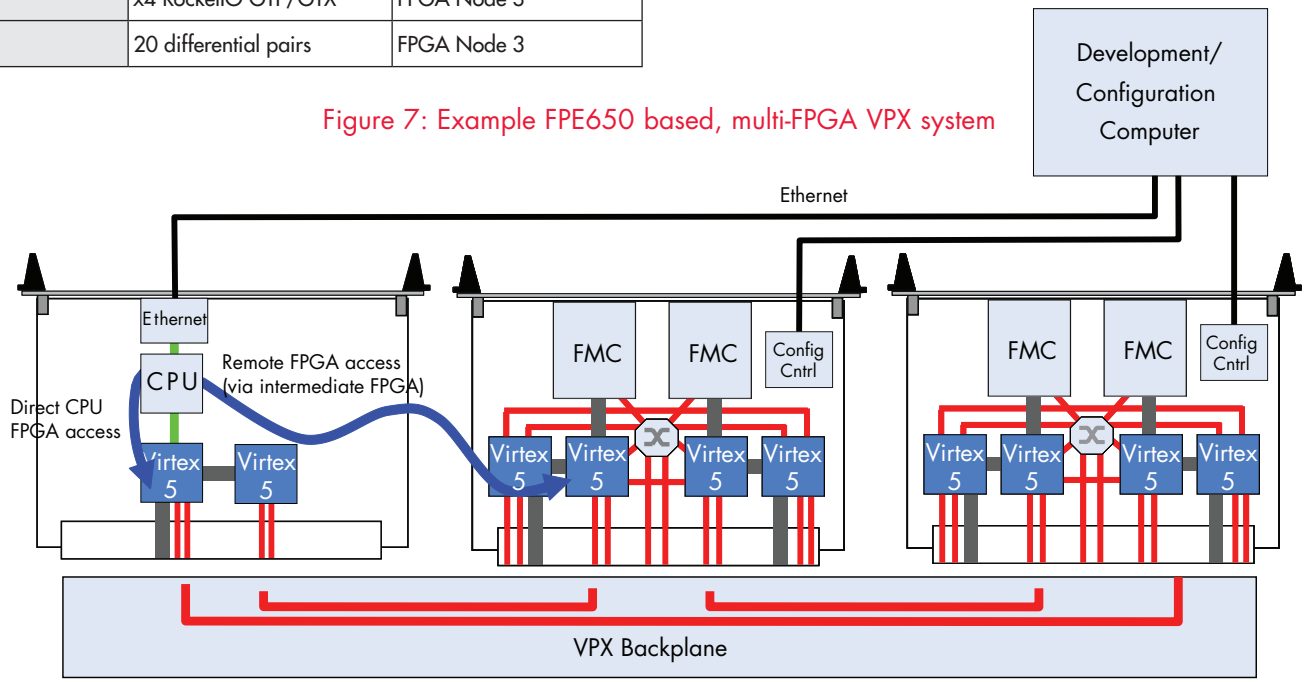
VPX (ANSI/VITA 46.0-2007) provides a large number of high-speed serial connections to the backplane. The FPE650 makes use of these connections to link all of the FPGAs to the backplane for direct parallel communications. The primary method for high-bandwidth off-board input/output is via the FPGA RocketIO transceivers, but parallel ports are also provided. All VPX links are AC coupled and are able to run at up to 3.125 GB/s per 1x link. See the Reference Clocks below for onboard clock sources.

Software/HDL Support

The FusionXF FPGA Development Kit provides examples and infrastructure for using and programming the FPE650 FPGAs. This is a common environment with other CWCEC Xilinx Virtex-5 and Virtex-4 based products.

One of the challenges in developing new HDL code and software with FPGA based products is creating drivers to work alongside the HDL IP. FusionXF is a framework for being able to incorporate new functionality or capabilities. This includes drivers for custom IP and the ability to bring them up in a controlled manner - and includes high-speed DMA driven interfaces. This makes development of IP easier and integration more straightforward. The FPE650 does not have an onboard CPU. However, in a typical system, there

Figure 7: Example FPE650 based, multi-FPGA VPX system





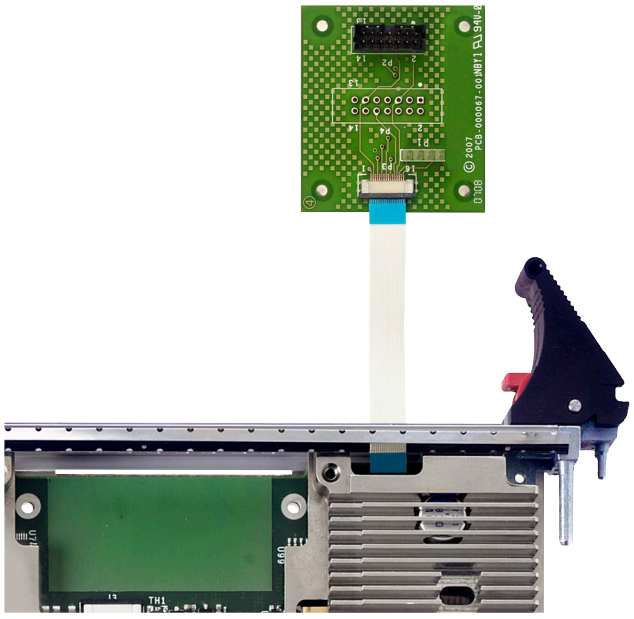
is usually a single board computer or host CPU to control boards such as the FPE650. FusionXF for other CWCEC boards include the ability for remote register access giving the host CPU access to all FPGAs in the array as if they were directly connected to the CPU - even though there may not be a direct link, but perhaps through an intermediary FPGA. This allows the driver structures to be extended across the system, including remote interrupts and register access.

Remote CPU based hosts are optional. The FPE650 can be used standalone or alongside other FPE650 FPGA boards. HDL examples with FusionXF illustrate how to interface and use external resources such as the QDRII SRAM and DDR2 SDRAM memory banks with high-performance DMA driven interfaces from the host.

For FPGA to FPGA communications, or Inter-FPGA Communications (IFC), FusionXF also includes components to simplify the development and use of RocketIO based data links. Support is included for independent data streams sharing physical interfaces and message forwarding to remote nodes via intermediate FPGAs when there is no direct connection. This makes system development using multiple FPGAs easier, faster and more reliable.

JTAG ports are provided by the FPE650 for use with ChipScope™/JTAG development tools. This is provided through a mini header. CWCEC provides an adapter module (JTAG-ZF5) for convenience. See Figure 8 (JTAG-ZF5 connected to an FPE650 below.

Figure 8: JTAG-ZF5 connected to an FPE650



FMC (FPGA Mezzanine Card)

FMC is an emerging standard being defined under the VITA 57 committee. The need for FMC has arisen because FPGA based I/O is different from conventional processors such as CPUs which use open standard bus based structures such as PCI-X. Often such interfaces are unsuitable for FPGA based I/O because they can slow the data interfaces and consume valuable FPGA resources. Since FPGAs are, by their nature, configurable they can adapt to a wide range of I/O structures -unlike CPUs. FPGAs are at their best when they are not treated by CPUs, but simply connect directly with the I/O device or port.

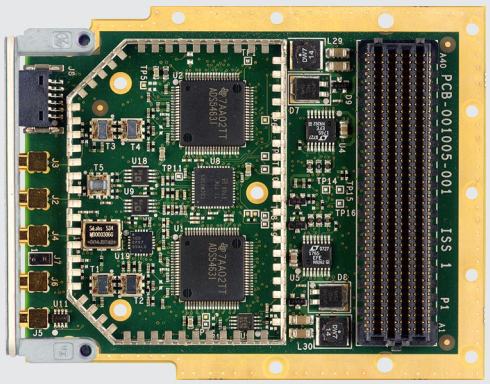
An FMC provides a large number of I/O connections to the host FPGA. This simplifies I/O mezzanine design, reduces cost and often make them higher performance solutions. Typical FMC modules comprise of the I/O device, such as an ADC (with front end signal conditioning), buffer and connectors - bus converters are unnecessary and become unnecessary overhead. An FMC can be used to provide analog I/O, digital I/O, fiber-optic interfaces, frame grabbers, additional memory or even dedicated DSP functions.

FMC modules are about half the size of PMC or XMC modules (similar width), but provide higher density host I/O.

Key FMC features include:

- Up to 192 differential pairs
- High-speed serial ports
- Air- and conduction-cooled variants
- Module size 69 x 76.5 mm

Figure 9: Example FMC module



Rugged Build Options

A range of environmental requirements are addressed by the FPE650; air-cooled benign, air-cooled extended temperature, air-cooled rugged and conduction-cooled. This is based on a 1" board pitch defined by VITA 48. Contact CWCEC for information about 0.8" build variants.

Software Radio

The FPE650, when fitted with analog FMC modules, is an ideal platform for the implementation of software radio applications. The Large FPGAs, bristling with DSP enhancements, can easily accommodate multiple parallel digital down converters (DDCs) for extracting channels (frequency bands) of interest; or the converse digital up converters to convert complex digital baseband signals to real passband signals for modulation onto direct digitally synthesized (DDS) carrier frequencies.

Developers can adapt commercial IP cores to suit their application, develop their own IP from scratch or purchase IP that has been specifically developed for the FPE650, directly from CWCEC. Currently, wideband DDCs supporting the ADC510, ADC511 and ADC512 are available.

Table 3: Specifications

FPGA Node 1 & 3	
Devices	Xilinx Virtex-5 SX95T (speed grade 2)
DDR SDRAM	2 banks of 128 M x 16-bit and 2 banks of 128 M x 24-bit
QDR SRAM	2 banks x 4 M x 18-bit
User Flash	128 MB per FPGA
Parallel I/O	20 differential pairs per FPGA (1 & 3 only) to VPX P3/P6 connector
FPGA Node 0 & 2	
Devices	Xilinx Virtex-5 SX95T (speed grade 2)
DDR SDRAM	N/A
QDR SRAM	4 banks x 4 M x 18-bit
Parallel I/O	108 single-ended signals between FPGA 0-1 & FPGA 2-3
FMC Sites	
FMC Site 1	FPGA Node 0 Host - 68 differential pairs - x4 multi-GB/s serial port - Ethernet (SerDes)
FMC Site 2	FPGA Node 2 Host - 68 differential pairs - x4 multi-GB/s serial port - Ethernet (SerDes)

Configuration & System Monitoring	
Flash Configuration	128 MB (FPGA configuration)
Control Port	Ethernet (FMC site or backplane) HTML browser interface
VPX/VPX-REDI	
Compliance	ANSI/VITA 46.0-2007 VITA 48.0
Board Pitch	1" (contact CWCEC for 0.8" variants)
Power Supplies	12 V, 5 V, 3 V 3, 3 V 3 Aux, VBAT (used for maintaining FPGA encryption keys)
OpenVPX Profile	SLT6-PER-1F
Software/HDL	
Host Drivers for Remote Host Processors	Wind River VxWorks, Linux
HTML Browser	Embedded processor HTML interface for FPGA configuration, crossbar switch configuration, temperature monitors, power supply sensors and flash programming
Software/HDL Examples	Memory interfaces, data streaming library
Miscellaneous	
LEDs (yellow)	- User programmable LEDs (2 per FPGA)
LEDs (red)	- FPGA not configured (1 per FPGA) - Configuration controller not configured - Fault detection
Power	TBD
Weight	1015 g air-cooled 1248 g air-cooled, 2nd level maintenance



Table 4: Environmental Specifications

Part Number Extension		Air-cooled			Conduction-cooled	
		Level 0	Level 100	Level 200 (Note 6)	Level 100	Level 200
Temperature	Operating (Air-cooled Note 4) (Conduction-cooled Note 7)	0 to +50°C	-40 to +71°C	-40 to +85°C	-40 to +71°C	-40 to +85°C
	Non-operating (storage)	-40 to +85°C	-55 to +125°C	-55 to +125°C	-55 to +125°C	-55 to +125°C
Vibration	Sine (Note 1)	2 g peak 15-2 k Hz	10 g peak 15-2 k Hz	10 g peak 15-2 k Hz	10 g peak 15-2 k Hz	10 g peak 15-2 k Hz
	Random (Note 2)	0.01 g^2/Hz 15-2 k Hz	0.04 g^2/Hz 15-2 k Hz	0.04 g^2/Hz 15-2 k Hz	0.1 g^2/Hz 15-2 k Hz	0.1 g^2/Hz 15-2 k Hz
Shock (Note 3)	Operating	20 g peak	30 g peak	30 g peak	40 g peak	40 g peak
Humidity	Operating	0-95% non-condensing	0-100% non-condensing	0-100% non-condensing	0-100% non-condensing	0-100% non-condensing
	Non-operating (storage)	0-95% non-condensing	0-100% condensing	0-100% condensing	0-100% condensing	0-100% condensing
Conformal Coat (Note 5)		No	Yes	Yes	Yes	Yes

Notes:
1. Sine vibration based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15-44 Hz, depending on specific test equipment.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Standard air-flow is 8 cfm at sea level. Some higher-powered products may require additional airflow. Consult the factory for details.
5. Conformal coating type is manufacturing site specific. Consult the factory for details.
6. This is a non-standard product. Consult factory for availability.
7. Temperature is measured at the card edge.

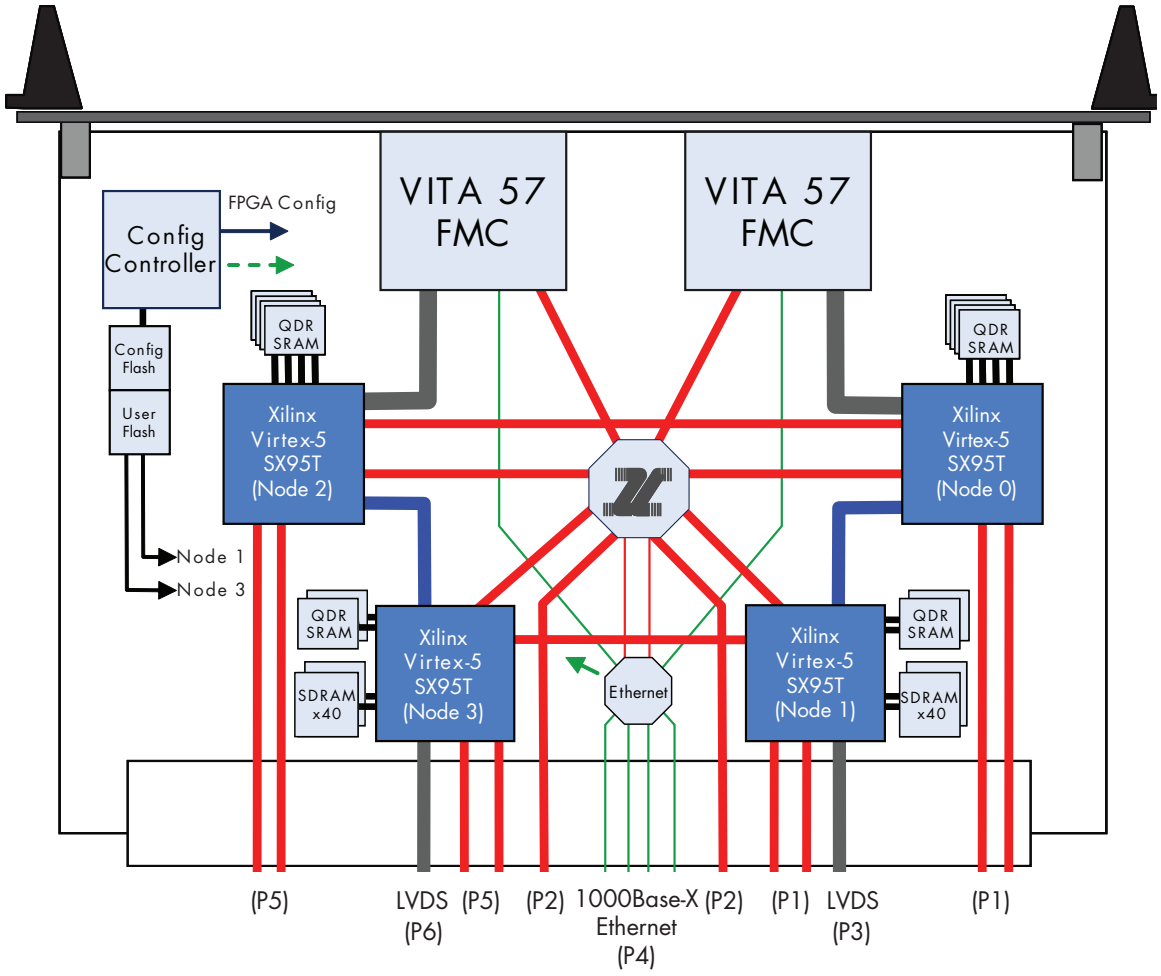
Table 5: Ordering Information

Part Numbers	Description	Environmental Level
FPE650-S04	Quad SX95T FPGA VPX, dual FMC site	Commercial build (AC Level 0)
FPE650-S04-B1H	Quad SX95T FPGA VPX, dual FMC site	Rugged air-cooled (AC Level 100)
FPE650-S04-D3H	Quad SX95T FPGA VPX, dual FMC site	Rugged conduction-cooled (CC Level 100)
FPE650-S05	Quad SX95T FPGA VPX (P2 connector removed), dual FMC site	Commercial build (AC Level 0)
FPE650-S05-B1H	Quad SX95T FPGA VPX (P2 connector removed), dual FMC site	Rugged air-cooled (AC Level 100)
FPE650-S05-D3H	Quad SX95T FPGA VPX (P2 connector removed), dual FMC site	Rugged conduction-cooled (CC Level 100)
FTM-01	Front panel breakout module (Ethernet)	
RTM01-C	Rear transition module (Ethernet)	
FPE650-XF	FusionXF support for FPE650	

Table 6: Compatible FMC Ordering Information

Suitable FMCs that can be used with the FPE650	
ADC510	Dual 500 MS/s 12b ADCs
ADC511	Dual 400 MS/s 14b ADCs
ADC512	Dual 3000 MS/s 8b ADCs
ADC513	Quad 1500 MS/s 8b ADCs
FMC-520	Quad 500 MS/s 16b DACs (Dual 1000 GS/s 16b DACs)
FMC-XCLK2	Multi-channel, low jitter clock generator

Figure 10: FPE650 block diagram



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

Technical Support

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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