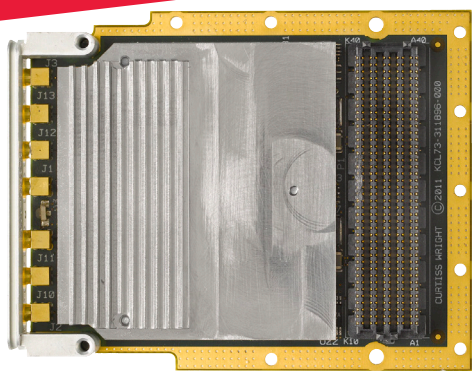
Fact Sheet

FMC-516

Quad-Channel 250 MSPS 16-bit Analog Input FMC



Applications

- Signal Intelligence (SIGINT)
- Electronic Counter Measures (ECM)
- Radar

Features

- Quad 250 MSPS 16-bit ADCs
- Onboard programmable sample clock
- FMC/VITA 57 form factor
- Air- or conduction-cooled rugged versions

Benefits

- Direct ADC connection to host FPGA ensures maximum throughput
- Able to synchronize multiple channels/ boards
- Easily interfaces to FPGA-based host board
- Digital receiver front end

Overview

The FMC-516 is a quad channel 250 MSPS 16-bit analog input FPGA Mezzanine Card (FMC). The FMC (VITA 57) specification allows I/O devices to be directly coupled to a host FPGA. This makes the FMC516 an ideal digital receiver front end. On the FMC-516, the four ADC devices connect through the high bandwidth FMC connector to an FPGA-based host board which maximizes data throughput and minimizes latency.

The FMC-516 supports an onboard programmable sample clock generator as well as an external reference input. Multiple FMC-516 boards can be synchronized to increase the number of input channels through the use of trigger input/output signals directly under the control of the FPGA. The FMC-516 can be used on platforms like Curtiss-Wright Controls Embedded Computing's VPX6-472 (MPC8641D/dual Xilinx Virtex-6), FPE650 (quad Xilinx Virtex-5), HPE720 (MPC8641D/dual Virtex-5) or FPE320 (Xilinx Virtex-5) which provides processor nodes for a powerful digital receiver platform.

Analog Input

The FMC-516 supports four analog inputs through 50Ω MMCX type front panel connectors. The analog inputs are single-ended and are coupled to Intersil ISLA216P25 ADCs using a balun and AC coupling capacitor configuration to produce the broadband differential input required by the devices.

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Clocks, Triggers & Synchronization

The FMC-516 ADC's sample clock can be driven from either an external source or onboard programmable sample clock generator. The clock source is controlled by the host FPGA.

The external front panel clock input is provided through an MMCX type front panel connector. The external clock source can be either a direct RF sample clock or external 10 MHz reference input. If the external 10 MHz reference is selected, then the sample clock is derived from the onboard programmable clock generator driven by the 10 MHz source. The minimum sample clock supported by the FMC-516 ADCs is 40 MSPS. The external sample clock is a 50Ω LVPECL input designed to operate with an input level between 0 dBm and + 8dBm. The clock input may be sinusoidal or square.

Trigger In and Trigger Out use MMCX type front panel connectors. The actual functionality of these signals is dependent on the HDL code in the FPGA of the host carrier card. Both 'Trigger In' and 'Trigger Out' are single-ended LVPECL buffered signals connected to the host FPGA. It is possible to synchronize the ADCs on multiple FMC-516s using the Trigger In & Trigger Out signals with appropriate HDL code; effectively the function of these signal is changed to a sync mode when this is required. For applications which do not require 'Trigger' capability, it is possible for user developed HDL to use these for other functions.

FusionXF Software/HDL Support

Curtiss-Wright's FusionXF development kit includes software, HDL and utilities with examples and infrastructure for using the FMC-516 on each supported host.

One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA. It facilitates the inclusion of signal processing blocks such as digital down converters, making HDL development easier and integration more straightforward.

Table 1: Specifications

Analog Input	
Number of Channels	4, single-ended
Sampling Frequency	Up to 250 MSPS
Full Scale Input Voltage	2V pk-pk
Device	Intersil ISLA216P25
Analog Bandwidth	100 MHz (3dB) 600 MHz (10dB)
SFDR (at 100 MHz)	82 dBFS
SNR (at 100 MHz)	72 dB
ENOB (at 100 MHz)	11.70 bits
Input Impedance	50 Ohm, AC coupled
Input Connector	Front panel MMCX
Clock & Trigger Inputs	
Clock Input Connector	Front panel MMCX
Clock Input	50 Ohm, AC coupled LVPECL
Clock Input Frequency	10 MHz (Reference) or 40-250 MHz (RF)
Internal Clock	Programmable (derived from 10 MHz external source or internal): Si571 VCXO
Trigger Input/Output	Single-ended, 50 Ohm, LVPECL buffered to host FPGA
Software/HDL	
Host HDL Code	Analog input hosted by FusionXF on Curtiss-Wright hosts. Including block & continuous capture (contact Curtiss-Wright for other hosts).
Environmental	
Ruggedization Levels	Air-cooled Air-cooled rugged L100 Conduction-cooled L200

Figure 1: FMC-516 Block Diagram