Data Sheet

CHAMP-FX3 (VPX6-472)

Xilinx® Virtex®-6 6U OpenVPX™ Module

Features

- 6U OpenVPX™ (VITA 65) profile MOD6-PAY-4FIQ2U2T-12.2.1-1, VPX REDI (VITA 48 option)
- Dual user-programmable Xilinx® Virtex®-6 FPGAs (SX475T or LX550T), each with:
  - 2 GB DDR3 SDRAM in two banks
    - Supports migration to 4 GB per FPGA
  - 72 MB QDRII+ SRAM in four banks
  - Four 5 GHz 4-lane serial links to the backplane
  - Three 5 GHz 4-lane serial links between the two FPGAs
  - One 4-lane Serial RapidIO® 1.3 link to the onboard switch fabric
  - 20 LVDS pairs to the backplane
  - 20 differential pairs between both FPGAs
  - FMC connection with 80 differential signal pairs
- Freescale™ Power Architecture™ MPC8640D processor
  - Running at 1 GHz
  - 1 GB SDRAM in two banks
  - 256 MB flash
  - Two Gigabit Base-T Ethernet links to the backplane P4 connector
  - Two Gigabit Base-X Ethernet links to the backplane P4 connector
  - Two RS-232 links to the backplane
- Two Mezzanine sites with support for FMC (VITA 57)
- Onboard sRIO 1.3 switch
  - Four 4-lane fabric ports to the backplane
  - 4-lane ports to both user FPGAs and the MPC8640D processor
- Thermal sensors for monitoring board temperatures
- Sensors for monitoring board power consumption
- Support for ChipScope™ Pro and JTAG processor debug interfaces
- Multi-board synchronous clock
- FusionXF BSP and FPGA design kit with highly-optimized IP Blocks, development environment, reference designs, scriptable simulation test benches and software libraries
  - VxWorks® and Linux® variants available
- Continuum IPC – inter-processor communications middleware available
- Continuum Vector subroutine library available
- VITA 48 1" pitch format
- Ruggedization levels
  - Level 0 (Commercial)
  - Air-cooled level 100
  - Conduction-cooled level 200

Learn More
Web / sales.cwcembedded.com
Email / sales@cwcembedded.com

ABOVE & BEYOND

CURTISS WRIGHT Controls
Embedded Computing
cwcembedded.com



Overview

The CHAMP-FX3 is a next generation module in Curtiss-Wright Controls Embedded Computing's family of user-programmable FPGA-based computing products, designed to meet the needs of challenging embedded high-performance digital signal and image processing applications. The CHAMP-FX3 combines the dense processing resources of two large Xilinx® Virtex®-6 FPGAs with a powerful AltiVec™-enabled dual-core Freescale™ Power Architecture™ MPC8640D processor, on a rugged 6U OpenVPX™-compatible (VITA 65) form factor module.

The CHAMP-FX3 complements this processing capability with a rich assortment of rear-panel I/O and memories, including a Serial RapidIO® (sRIO)-based switching fabric, multiple high-speed serial links, and 20 pairs of LVDS links to the backplane that can be used to support Camera Link or other high-speed parallel interface. There are also two FMC sites that have been enhanced to support the next generation of FMC cards with 80 pairs of differential signals.

This combination of enormous processing density and I/O flexibility make the CHAMP-FX3 an ideal choice for many commercial or rugged embedded applications including radar and signal intelligence, and Intelligence, Surveillance and Reconnaissance (ISR) platforms. The CHAMP-FX3 is supported by the FusionXF Suite, which provides infrastructure and support for HDL development, software, and multi-processing applications, including sRIO. VxWorks® and Linux® are supported operating systems for the MPC8640D.

Xilinx Virtex-6 FPGAs

At the heart of the CHAMP-FX3 are two Xilinx Virtex-6 FF1759 package FPGAs, the largest FPGAs in the Virtex-6 LXT and SXT families, which have high-speed SerDes. FPGAs provide parallel processing capabilities, reducing processor count and system size. Operations such as FFTs, FIR filters and other fixed-point and/or repetitive processing tasks are highly suited for placement inside FPGAs. The two large FPGA nodes can process input from the two FMC mezzanine sites or backplane I/O, or can simply function as additional compute resources to the general purpose system processor. The FPGA nodes on the CHAMP-FX3 support device families from the Xilinx Virtex-6 family, specifically the SX475T and LX550T. By using the LXT for logic-intensive applications and the SXT for DSP applications, developers can tailor their hardware resources to match their algorithm needs. (See the CHAMP-FX3 FPGA Resource Table). The SX475T and LX550T devices. With over 550,000 logic cells, the LXT family gives FPGA designers the most amount of space to program their algorithm. With 2,016 DSP slices and over 475,000 logic cells, the SXT device is ideal for A/D intensive projects where the DSP48E slices can be used to maximum benefit. Note that initially only the SX475T variant will be offered for development systems.

Larger Chips Reduce Development Time

The use of large FPGA nodes simplifies algorithm development, as processing can be done inside a single device or a reduced number of devices. When compared with the smaller package FPGAs, larger FPGAs have more logic slices available. The availability of more logic gives

Table 1: CHAMP-FX3 FPGA Resource

	Logic Resources			Memory Resources			Clock Resources	Embedded Hard IP Resources & Speed Grades			
	Slices	Logic Cells	CLB Flip-Flops	Max. Dist. RAM (kbits)	Block RAM/ FIFO w/ ECC (36 kbits each)	Total Block RAM (kbits)	Mixed Mode Clock Manager (MMCM)	DSP48E Slices	PCIe Endpoint Blocks	Speed Grade*	RocketIO GTX* (run at 5.0 GHz or lower)
LX550T	85,920	549,888	687,360	6,200	632	22,752	18	864	2	-1C, -1I**	36
SX475T	74,400	476,160	595,200	7,640	1,064	38,304	18	2,016	2	-1C, -1I**	36

Notes
*These features are specific to using the FPGAs on the CHAMP-FX3 and do not reflect all of the capabilities of the FPGAs themselves.
** -1I part used on rugged boards

designers greater freedom, making timing easier to close, and hence shortening development cycles. Additionally, as more FPGAs are used, greater complexity is needed to partition the algorithm and link the devices together. These I/O resources come at a greater expense in smaller devices, which already have less logic. When combined with a large amount of memory and I/O resources, the larger devices can fulfill processing needs for a variety of applications while still easing customer development. Since Xilinx does not offer -2I parts in the largest size, -1C and -1I parts are used to provide a similar speed performance across non-rugged and rugged variants. This helps ensure that applications which run across a L0 temperature range on a commercial grade module will also pass when run over extended temperatures on a rugged module.

FPGA Architecture

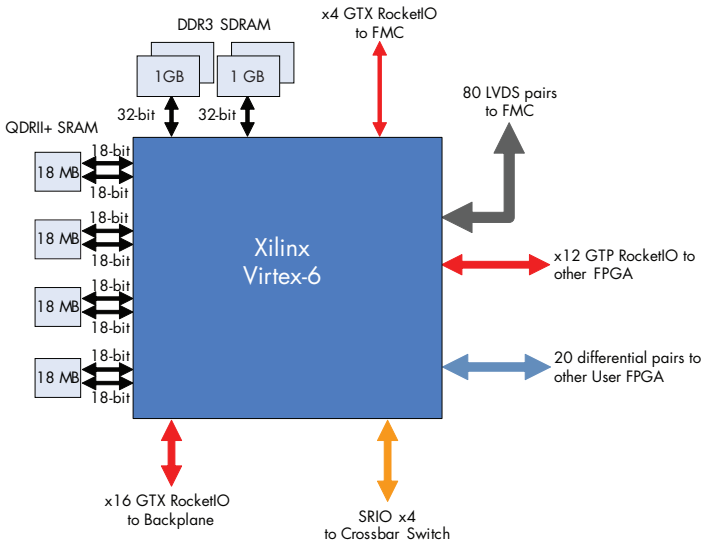
The FPGA nodes on the CHAMP-FX3 have industry leading I/O and memory resources to maximize the effectiveness of the devices in a variety of applications.

Memory

The memory resources on each FPGA node of the CHAMP-FX3 give users the ability to process and store data sets for the most demanding applications. Each FPGA node has both DDR3 and QDR-II+ SRAM available. The DDR3 is organized into two banks, with each bank providing a x32 bus width using four x8 devices. Up to 2 GB of memory is available (1 GB initially with 2 Gb parts) from each DDR3 bank, providing a large amount of storage space for data sets. The clock frequency of the DDR3 interfaces is 400 MHz, pending characterization, giving an expected maximum throughput of 3.2 GB/s in a given direction, per bank.

For more processing-intensive tasks, four independent banks of QDR-II+ SRAM complements the DDR3. The banks each have two x18 ports (one read, one write) and provide significant bandwidth as they are double data rate (DDR) interfaces. Each bank is 18 MB, for a total of 72 MB available from each FPGA. The clock frequency of the QDRII+ interface is 350 MHz, pending characterization, giving an expected maximum throughput of 1.4 GB/s in both directions simultaneously, per bank.

Figure 1: FPGA Memory & I/O



FPGA I/O

The FPGA nodes on the CHAMP-FX3 have an ample amount of I/O resources for connecting to other parts of the system. In terms of RocketIO™ high-speed serial links (GTX), the FPGA nodes have utilized the maximum available GTX links (36) for the device selected on the CHAMP-FX3. These links are divided between I/O to the mezzanines, between the two FPGAs, to the backplane, and the sRIO fabric. The GTX interfaces are supported up to a maximum frequency of 5.0 GHz, pending characterization. Parallel I/O is also used, with 80 differential pairs routed to the local FMC site, 20 differential pairs routed to the backplane, and 20 differential pairs routed to the other FPGA. While the FMC and backplane signals are typically configured as LVDS, the inter-FPGA signals are SSTL15 due to the FPGA bank where the signals are located.

MPC8640D Power Architecture Processor

Dual CPU Cores

The Freescale MPC8640D forms a fully integrated processor node with dual CPUs, memory controllers, DUART, Ethernet controllers, PCIe and sRIO. The e600 Power Architecture CPU cores include floating-point units for high-performance DSP processing. The processor core frequency is 1.0 GHz. Each core has access to board management functions (temperature sensors, RTC and voltage monitors).

Memory

The MPC8640D has two integrated memory controllers. Each controller supports 512 MB of DDR2 SDRAM memory for a total of 1 GB. The memory is configured as 64-bit data and 8-bit ECC, operating at 200 MHz. The peak total memory bandwidth is 3.2 GB/s. Each e600 core has its own 1 MB L2 cache.

Flash

There is a total of 256 MB of flash that can be split between two banks or used as one larger bank. The flash can be used for non-volatile storage of the CHAMP-FX3's bootloader, applications and FPGA configuration images. The CHAMP-FX3 has a switch to protect the bootloader image and/or data from being accidentally overwritten.

Board Connectivity

Serial RapidIO Infrastructure

An 8-port, Generation 1.3 sRIO switch connects the MPC8640D processor, both Virtex-6 FPGAs, and provides four connections to the backplane through the P1 VPX connector. Each connection has four lanes, with each lane running at 3.125 GHz. The sRIO infrastructure can be used to connect with other Curtiss-Wright boards, including the CHAMP-AV6, CHAMP-AV8, VPX6-185, CHAMP-FX3 and MFC700.

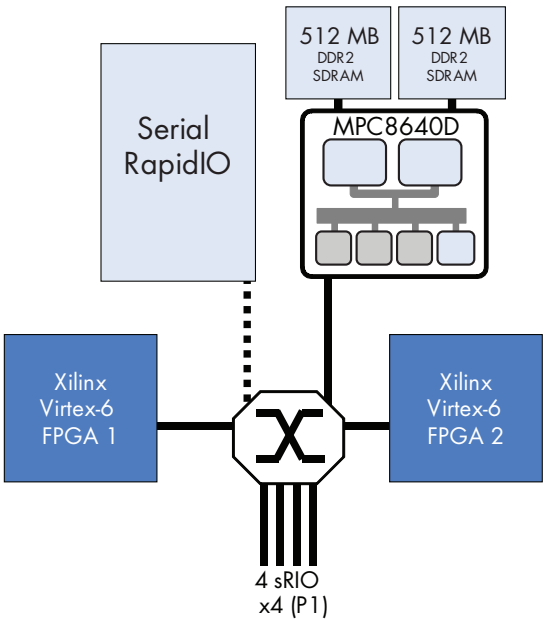
PCI Express

There is a PCIx8 connection from the MPC8640D processor to the P5 VPX connector.

Ethernet

There are 2 GbE Base-T connections to the rear panel P4 connector, and 2 GbE Base-X connections to the rear panel P4 connector. All Ethernet connections are supported by the MPC8640D processor. The Base-T connections are available off the RTM break-out cable.

Figure 2: Serial RapidIO Infrastructure



Serial I/O

The CHAMP-FX3 has two UART ports connected to the MPC8640D. An EIA-232 connection is available through the backplane via a breakout cable on the RTM.

Cabling

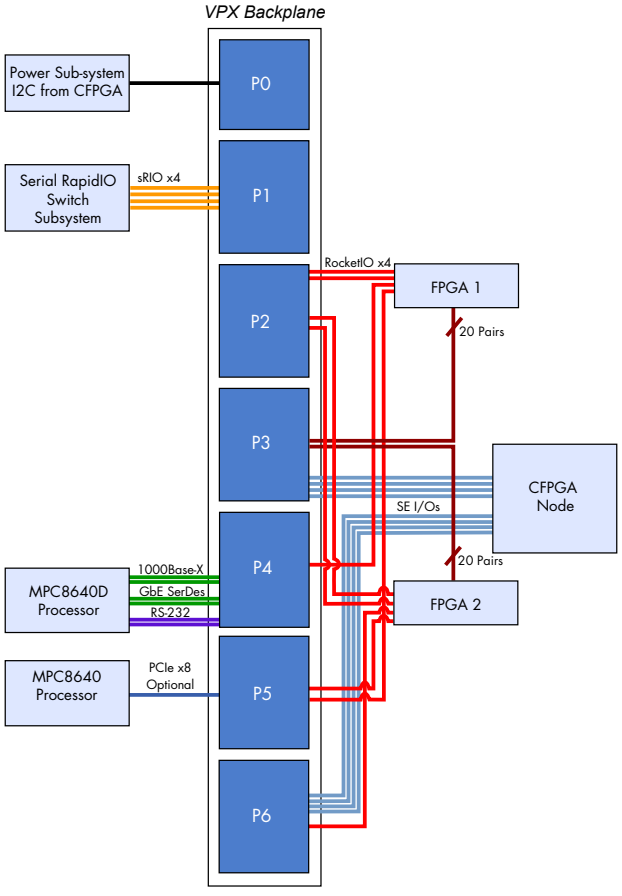
A break-out cable connecting to the rear panel connector via an RTM provides access to two EIA-232 connections, 1 GbE connection, JTAG and a reset button.

Configuration FPGA & Chassis Management

The onboard Configuration FPGA Node (CFPGA) controls chassis management, power and temperature monitoring, bit-stream encryption, and other general board support functions. The CFPGA is controlled by the MPC8640D's local processor bus.

The following figure shows the backplane connectivity for the module.

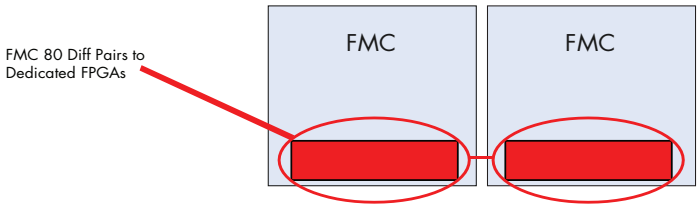
Figure 3: Backplane Connectivity



Mezzanine Sites

The CHAMP-FX3 includes a versatile set of I/O options through dual FMC sites. The dual FMC sites provide flexibility for the latest I/O such as A/D converters, sFPDP, LVDS, and Fibre Channel, but also allows support for legacy I/Os. The board can be used as a front-end solution to stream in data using the dual mezzanine sites for inputs, before passing data forward for further processing using sRIO or other high-speed interconnects. For space constrained applications, the board functions as a system-onboard, providing the ability to input and output data in a single-slot with two mezzanines.

Figure 4: Mezzanine I/O Support



FMC Site

The VITA 57 FPGA Mezzanine Card (FMC) sites utilize 160 user I/O pins from the dedicated FPGA nodes:

- LA[00-33]_P/N = 34 differential pairs/68 single-ended with DCI termination
- HA[00-23]_P/N = 24 differential pairs/48 single-ended with DCI termination
- HB[00-21]_P/N = 22 differential pairs/44 single-ended with DCI termination

Customer developed, third party, or Curtiss-Wright FMC modules can be used with the CHAMP-FX3. Announced FMC products from Curtiss-Wright include analog I/O boards which can be used to tailor the I/O capabilities of the CHAMP-FX3 to customer project specific needs.

Using the CHAMP-FX3 along with Curtiss-Wright's Signal Acquisition FMC cards such as the ADC512/ADC513 provides a complete Digital Receiver Solution. Since FMCs have no FPGA on them and are lower power, they are better able to handle extreme rugged conditions. Furthermore with the flexibility of the FMC interface, alternate front ends can be accommodated by using different FMC modules.



Software and HDL

Board Support Packages

The CHAMP-FX3 can be delivered with Wind River VxWorks or Wind River GPP Linux Board Support Packages (BSPs). VxWorks 6.7 will be supported in initial release, migrating to VxWorks 6.9 in 1.1 release. Wind River Linux GPP 3.0 will be supported. The BSP is accompanied by a bootloader which contains the necessary drivers for enumerating and enabling all onboard hardware devices, such as memories, bridges, and Ethernet controllers. The bootloader is responsible for booting the operating system. The BSP also contains a number of useful functions and drivers for flash programming, debugging, real time clock management, watchdog timers, etc. Initial release will be AMP, while SMP will be supported by 1.1 release.

FusionXF FPGA Development Kit

FusionXF provides FPGA HDL functions, application APIs, drivers, and utilities to simplify the task of integrating FPGAs into an embedded real-time DSP system design. It aids customers in the development of their FPGA algorithms and logic for Curtiss-Wright customer- programmable FPGA products. All the building blocks are provided to build a fully functional FPGA design into which a customer can integrate its FPGA logic and algorithms. It provides mechanisms for communication between FPGAs as well as communication between FPGAs and processors. Also included in the Kit are example designs that show how to implement common FPGA functions such as control registers, DMA engines and interrupts, and how to control these functions and communicate with them from software. FusionXF is comprised of a Hardware Development Kit (HDK) and Software Library.

FusionXF contains software libraries, drivers, and utilities for use in VxWorks and Linux environments to facilitate the initialization and control of FPGAs, and to communicate and move data between FPGAs and application software. Software drivers and libraries are provided to allow processing nodes to utilize FPGAs as co-processors, DMA engines, and memory pools. Utilities are provided to perform functions such as loading new images into the FPGA's flash memory.

FMC (VITA 57)

Traditional open standard bus-based structures like PCI-X are less suitable for FPGA I/O, because they can slow data transfer rates while consuming valuable FPGA resources. FPGA I/O is inherently configurable and can be adapted to a wide range of I/O structures. FPGA I/O is best optimized when FPGAs are not treated the same way as CPUs, rather are connected directly with I/O devices or ports. The VITA 57 FMC open standard has been developed to capitalize on these FPGA attributes.

The FMC standard provides an industry standard mezzanine form factor in support of a flexible, modular I/O interface to an FPGA located on a baseboard or carrier card. It allows the physical I/O, interface to be physically separated from the FPGA design while maintaining a close coupling between a physical I/O interface and an FPGA through a single connector, P1.

There is a choice of two very high-bandwidth connectors to interface the FMC to an FPGA on a carrier: a Low Pin Count (LPC) connector with 160 pins and a High Pin Count (HPC) connector with 400 pins. An FMC with the LPC connector can mate with a carrier that utilizes either an LPC or HPC connector.

The use of the FMC standard simplifies FPGA designs, reduces cost, and makes the design of I/O mezzanine modules simple and straightforward. Development cycles can be shortened and costs lowered by utilizing a single FPGA design in multiple applications, by simply mounting different FMC modules.

Typical FMC modules will have an I/O device, such as an ADC (with front end signal conditioning), buffer and connectors. Since FPGAs can interface directly to I/O device pins, there is no need for any bus interfaces like PCI. Therefore bus converters are unnecessary overhead that can be left out of the design.

FMCs can be used to provide analog I/O, digital I/O, fiber-optic interfaces, camera interfaces, frame grabbers, additional memory or even dedicated DSP functions.

FMC modules are of a similar width, but half the size of PMC or XMC modules, but provide higher density host I/O.

Key FMC features include:

- Up to 192 differential I/O pairs
- Up to 10 high-speed serial I/O links
- Air and conduction-cooled variants
- Module size of 69 x 76.5 mm

The FusionXF HDK contains HDL functions that are common to most FPGA application, such as DDR3. There are HDL functions provided such as DDR3 and QDRII+ memory controllers, RocketIO interfaces, parallel I/O interfaces. Commonly used FPGA functions are included, such as DMA engines and register sets. In addition, there are HDL functions provided to implement protocols such as PCIe and sRIO. The hardware independent HDL code resides in the VM Library. The hardware dependent HDL code resides in the BSIP. See Toolkit Datasheet for more information.

IPC Development Kit

IPC provides Inter-Processer Communication (IPC) capabilities targeted at Distributed Multiprocessing (DMP) applications. It provides a simple, yet high-performance, low latency mechanism for bulk data transfers between distributed processors. IPC consists of a IPC driver that provides peer-to-peer communication capabilities between processors over a system interconnect fabric, and a IPC library that provides POSIX APIs.

IPC is based on a Shared Memory Buffer (SMB) communication approach that is independent of the lower layer transport protocol. The first transport protocol supported by IPC is sRIO.

Figure 5: FusionXF & IPC

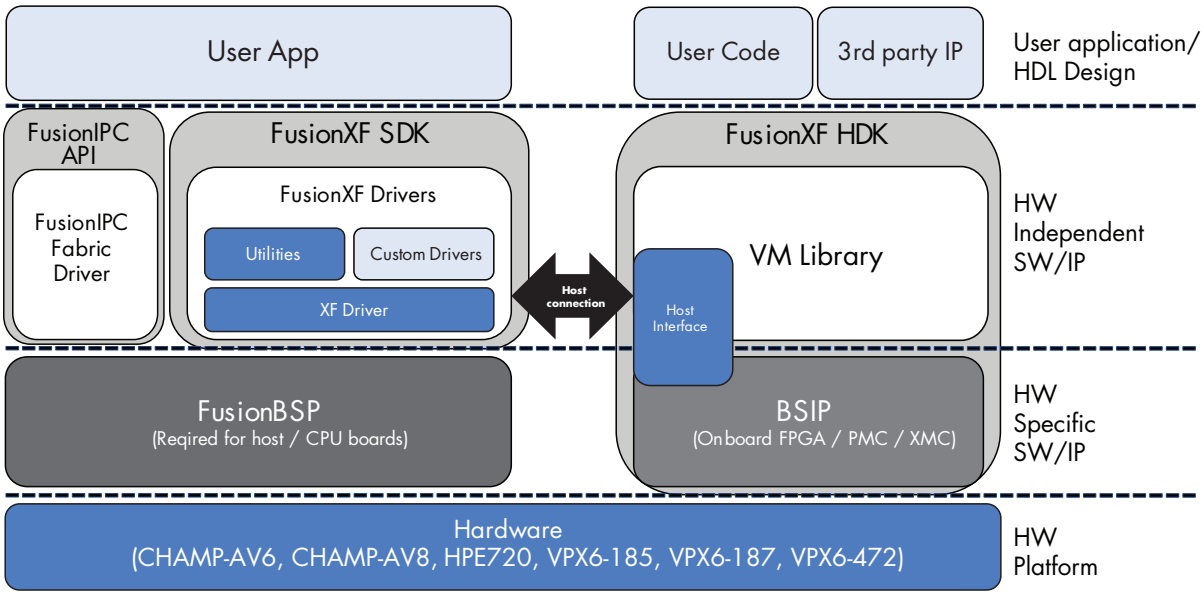




Table 3: Specifications

FPGA	
Device	Xilinx Virtex-5, SX475T, LX550T
No. of FPGAs	2
Memory (per FPGA)	◆ 4x 18 MB QDRII+ SRAM (18-bit data paths) ◆ 2x 1-2 GB DDR3 SDRAM (32-bit data paths)
Connectivity	◆ x16 GTX RocketIO per FPGA to backplane (5 GHz) ◆ P2 (Expansion Plane) – x8 from each FPGA ◆ P5 – x4 from each FPGA ◆ P4/P6 – x4 from FPGA 1 and FPGA 2 respectively ◆ x12 GTX RocketIO between FPGAs (5 GHz) ◆ x4 GTX to dedicated FMC site from local FPGA ◆ x4 sRIO to crossbar switch ◆ 20 differential pairs to backplane
Configuration	JTAG, MPC8640D processor via CFPGA, using onboard flash or SDRAM for bitfile storage
Power Architecture CPUs	
Device	Freescale MPC8640D
CPU cores	2, e600
Speed	1.0 GHz
Memory	64 KB L1 cache per core, 1 MB L2 cache per core (inc. ECC), 512 MB DDR2 per bank
Flash	256 MB
NvSRAM	128 KB
Mezzanine Sites	
FMC/VITA 57	Quad RocketIO x1 and 80 differential pairs
Ethernet	
Backplane	◆ Dual 1000Base-T to P4 Connector ◆ Dual 1000Base-X to P4 Connector
Device	Embedded within MPC8640D
Speed	10/100/1000 MB/s
PCI Express	
Connectivity	Backplane (x8 on P5), all at 2.5 Gb/s
Serial RapidIO	
Switch Device	IDT TSI578 8-port sRIO switch
Connectivity	Both FPGAs, MPC8640D, 4 connections to P1 fabric connector, all lanes at 3.125 Gb/s
Serial I/O	
Device	DUART embedded within MPC8640D
Backplane	Dual EIA-232 to P4

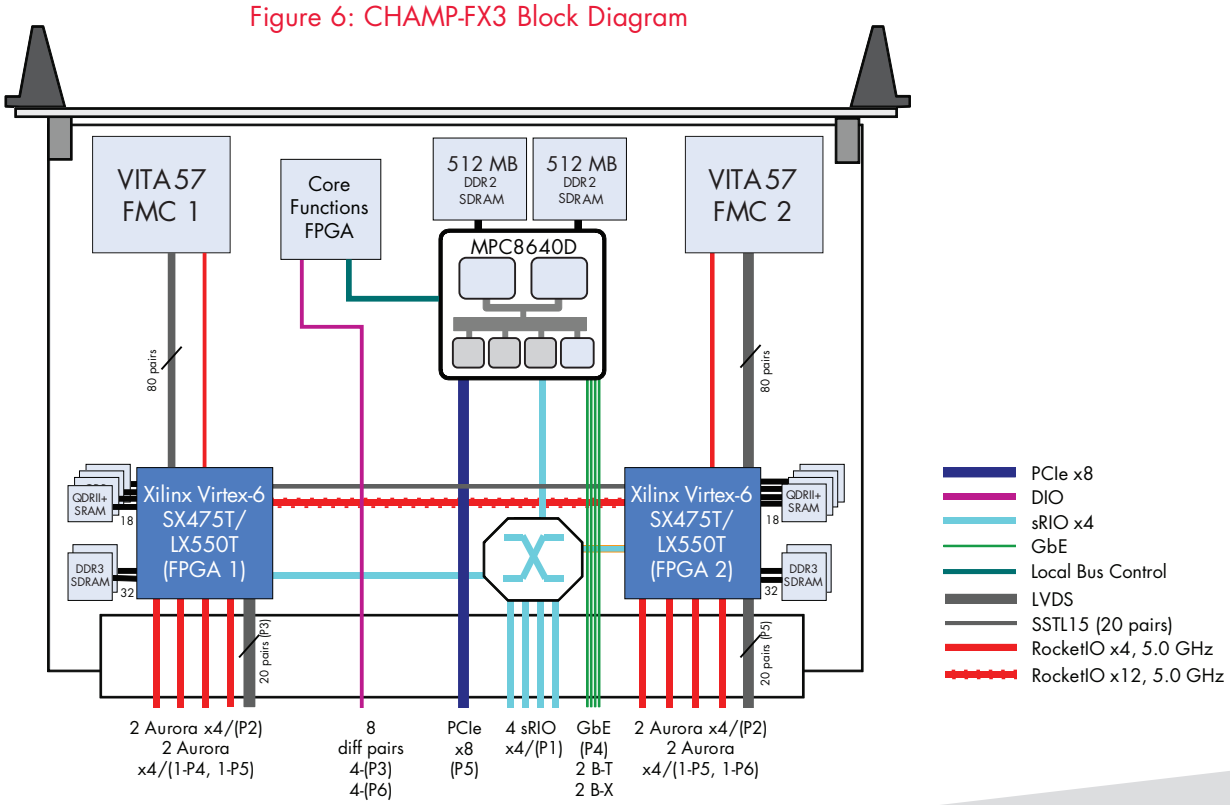
Backplane	
Compliance	◆ VPX (VITA 46) and VPX REDI (VITA 48) ◆ OpenVPX SLT6-PAY-4F1Q2U2T-10.2.1 ◆ OpenVPX MOD6-PAY-4F1Q2U2T-12.2.1-1 (if PCIe core in FPGA; else uses Aurora for expansion plane)
Connectivity	
P0	Power and CFPGA utility signals (I2C)
P1	4 sRIO x4 to switch
P2	2 RocketIO x4 to FPGA 1 and 2 RocketIO x4 to FPGA 2
P3	20 differential pairs to FPGA 1, 4 DIO from CFPGA
P4	4 GbE, 1 x4 RocketIO to FPGA 1
P5	1 x4 RocketIO from each FPGA, 20 differential pairs to FPGA 2, x8 PCIe
P6	1 x4 RocketIO to FPGA 2
Processor Local Bus	
Connectivity	32-bit wide connection from CPU to CFPGA
System Control Node	
Device	Xilinx Virtex-5 LX110
Connectivity	◆ 32-bit wide connection to MPC8640D ◆ Dual I2C buses ◆ 8 single-ended connections to P3 ◆ 8 single-ended connections to P6 ◆ 8 differential pairs to FPGA
Software/HDL Code	
Operating System	◆ VxWorks 6.7 (6.9 in release 1.1) ◆ Linux 3.0 (MPC8640D CPUs)
Utilities	Flash programming, diagnostics
HDL Code	FusionXF FPGA Development Kit, IPC Development Kit and U-Boot
Standards	
Compliance	VITA 20, 46.0, 46.3, 46.9, 48, 65 and IEEE 1386
Miscellaneous	
Power (estimated)	◆ 5 V (0 W) ◆ +12 V (typical 85 W, max 140 W at 85 °C, full load) ◆ Max expected power permitted per FPGA is 25-30 W (estimated)
Cabling	◆ Break-out cable with 4x EIA-232 connections, dual GbE, JTAG & Reset button (CABLE-1002) ◆ CBL-472-SFP-001 required for access to Rocket links via RTM. One cable per connector.
Weight	◆ Air-cooled: (estimated) 2.6 lbs (1.18 kg +/- 100 gm) ◆ Conduction-Cooled: (estimated) 3.3 lbs (1.48 kg +/- 100 g)
RTM	RTM6-472-000 and CABLE-1002 required with CHAMP-FX3. The RTM provides access to serial ports/ENET/RIO/JTAG/RST.

Table 4: Environmental Specifications

		Commercial	Rugged	
			Air-cooled	Conduction-cooled
			Level 100	Level 200
Part Number Extension[1]		-	B1H	D5H
Temperature	Operational (at sea level)	0°C to +55°C (15 CFM air flow)[2]	-40°C to +71°C (20 CFM air flow)[2]	-40°C to +85°C (card edge temp)[3]
	Non-Operational	-40°C to +85°C	-50°C to +100°C	-55°C to +100°C
Vibration	Operational (Random)	-	0.04 g^2/Hz	0.1 g^2/Hz
Shock	Operational	-	20 g peak, 11 ms half sine	40 g peak, 11 ms half sine
Humidity	Operational	5-95% non-condensing	Up to 95%	Up to 95%
Altitude [4]	Operational	-	-15,000 to 60,000 ft	-15,000 to 60,000 ft
Conformal Coating [5]		No	Yes	Yes

Notes
1. Availability of the ruggedization levels are subject to qualifications for each product.
2. For operation at altitudes above sea level, the minimum volume flow rate shall be adjusted to provide the same mass flow rate as would be provided at sea level. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat. Some higher-powered products may require additional airflow.
3. The contacting surface on the rack/enclosure must be at a lower temperature to account for the thermal resistance between the plug-in unit and rack/enclosure.
4. Depending on the technology used, the risk for Single Event Upsets will increase with altitude.
5. Coated with Humiseal 1B31 or 1B73EPA. (ref. http://humiseal.com for details)

Figure 6: CHAMP-FX3 Block Diagram





Part Numbers

Check with a Curtiss-Wright Controls Embedded Computing representative for availability of specific part numbers.

VPX6 - 472 - U V W X Z Z Z

- Build Options:
  - 0ZZ: Standard Product
  - 9ZZ: Customer Specific
  - XX0: Dual FMC
- FPGA:
  - 0: LX550T
  - 1: SX475T
  - 9: Custom configuration
- Mechanical Format:
  - 4: 1" pitch, no 2-level maintenance support
  - 5: 1" pitch, 2-level maintenance support (covers)
- Temperature Range:
  - 0: 0 to 50°C
  - 1: -40 to 71°C
  - 2: -40 to 85°C
- Cooling Method:
  - A: Air-cooling
  - C: Conduction-cooling
- Model Number
- Standard Prefix for 6U VPX cards

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

Technical Support

For technical support:

Website: www.cwcembedded.com/support

Email: support1@cwcembedded.com

The information in this document is subject to change without notice and should not be construed as a commitment by Curtiss-Wright Controls Embedded Computing. While reasonable precautions have been taken, Curtiss-Wright assumes no responsibility for any errors that may appear in this document. All products shown or mentioned are trademarks or registered trademarks of their respective owners.