

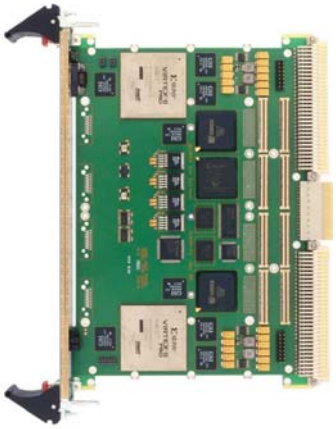
PRODUCT DATASHEET

CHAMP-FX

FPGA Accelerator Signal Processing Platform

Features

- 6U VME FPGA Accelerator signal processing platform
- Two user-programmable Xilinx Virtex-II Pro™ Platform FPGAs (XC2VP70 - XC2VP100)
- 512 Mbytes DDR266 SDRAM
- 18/36 Mbytes DDR II SRAM
- Two IBM 405 PowerPC™ processors per FPGA
- Two PMC/XMC (VITA 42) mezzanine sites with Processor PMC compatibility
- VITA 41 (VXS) and VME64x compliant with 8 serial links (up to 3.125 Gbps) to VITA 41 P0
- 8 bi-directional RocketIO™ ports to optional front-panel connectors
- Thermal and power management
- Two StarFabric interfaces for system level connectivity
- 64 Mbytes Flash memory for FPGA configuration files and processor code storage with a write protection feature
- Support for ChipScope Pro and JTAG processor debug interfaces
- *CHAMPTools-FX* FPGA design kit offers VHDL libraries, development environment, reference designs, simulation testbenches, and software libraries
- Range of air- and conduction-cooled ruggedization levels available



Overview

The CHAMP-FX is a reconfigurable computing platform targeted at replacing DSP, ASIC or processor farms in applications such as imaging, radar, data compression and signal intelligence. Algorithms such as FFTs and filters on incoming data streams have proven to be significantly more effective in FPGAs. FPGA technology allows unequaled parallelism and enables pipeline processing, typical in DSP applications. This card is well suited to front-end system processing, where sustained data rates and processing performance are important to overall system performance. Benefits include overall slot reduction, increased processing density and system cost reduction.

The CHAMP-FX provides an FPGA processing platform with a balanced mix of mezzanine interfaces, high bandwidth I/O, a variety of Double Data Rate (DDR) FPGA memories, off-board fabric connectivity and FPGA processing resources. The 6U VME-compatible card features two Xilinx Virtex-II Pro platform FPGAs (XC2VP70 - XC2VP100) for user-defined functionality. The card architecture provides a flexible standalone or system-level platform for solving a variety of signal processing challenges. The CHAMP-FX is designed to operate in rugged environments and is available in air- and conduction-cooled formats.

Thermal and power management of FPGAs is a critical factor when designing with large FPGAs. The CHAMP-FX provides the ability to monitor the FPGA die and board temperatures as well as the amount of current consumption of each FPGA through the user interface. The CHAMP-FX supports a flexible FPGA configuration manager. This allows the designer to store multiple FPGA configuration files in Flash or SDRAM memory. The ability to store configuration files in volatile memory is useful for fast FPGA reconfiguration and storage of classified data or algorithms. Each FPGA may be easily reconfigured with alternate configuration files via commands from a remote StarFabric node or the on-board user interface in under 100 ms.

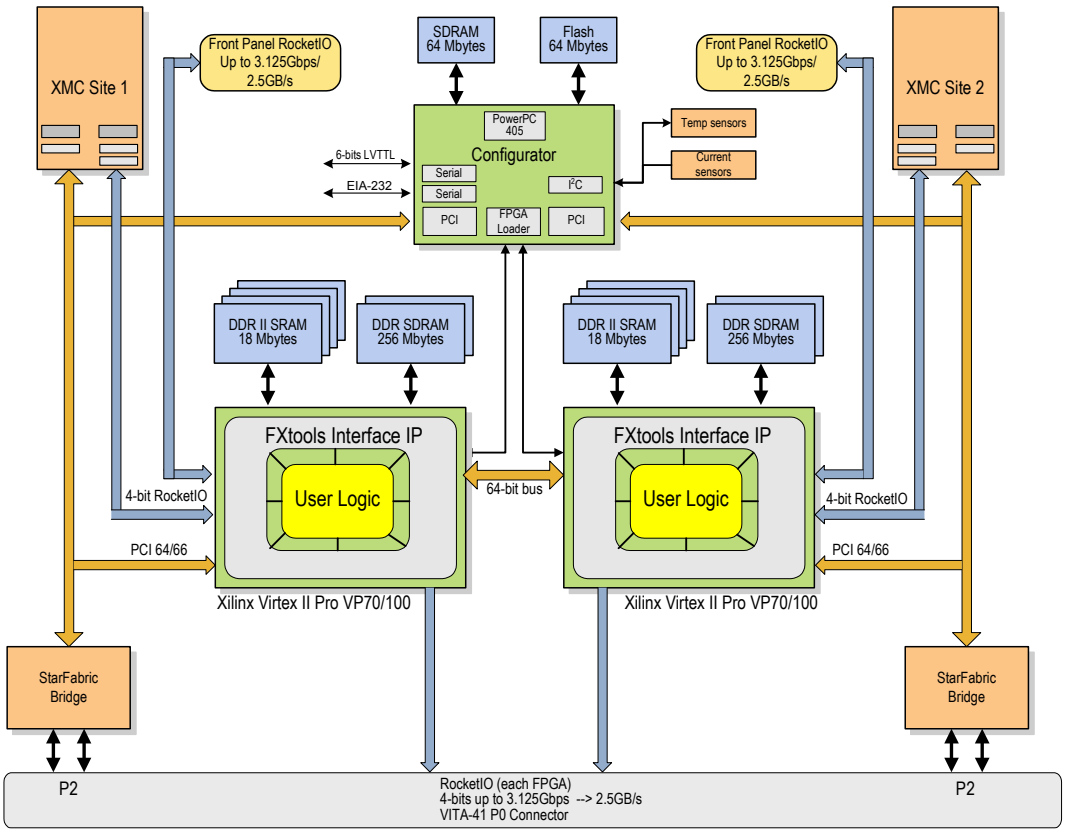
The *CHAMPTools-FX* FPGA design kit enables rapid prototyping of FPGA-based systems. A library of VHDL IP includes memory controllers, an initiator/target PCI interface and DMA controllers. The CHAMP-FX also enables the use of IBM CoreConnect™ internal SoC buses and miscellaneous Xilinx DSP functions. Also included are design templates, example designs, a VHDL testbench and Built-In Test (BIT) software. The CHAMP-FX provides a JTAG header on-card allowing the use of Xilinx ChipScope Pro and JTAG development tools. Refer to the *CHAMPTools-FX* datasheet for more details.

Architecture

The CHAMP-FX architecture is suited to DSP applications that place a high premium on sustained I/O mezzanine throughput, FPGA memory bandwidth and off-board fabric connectivity. The data flow capabilities of the CHAMP-FX ensure that applications can extract the most from the raw computing performance of the two Virtex-II Pro platform FPGAs. The CHAMP-FX architecture encompasses three key attributes that contribute to maximizing DSP performance:

- Two Virtex-II Pro platform FPGAs (XC2VP70 - XC2VP100)
- 8 GB/s peak FPGA memory bandwidth using two DDR SDRAM banks and four DDR II SRAM banks
- High-speed off-card I/O options include PMC/XMC sites, up to 10GB/sec of high-serial RocketIO and four StarFabric ports

Figure 1: CHAMP-FX Block Diagram



Operational Modes

Depending on system processing requirements, the CHAMP-FX may be used alone or in conjunction with other system elements. The CHAMP-FX supports three modes of operation:

- Standalone: Does not require other cards in the system for initialization, configuration, development or deployment. The *Configurator* FPGA executes code from flash memory and performs all board-level control and status functions.
- System implementation: The card is combined with other CHAMP-FX cards or our StarFabric products such as the CHAMP-AV/StarLink combination or the StarReach PMC carrier. The CHAMP-FX may be managed locally, or remotely by a dedicated processor in the StarFabric.
- Processor PMC implementation: A processor PMC may be used on the CHAMP-FX to provide local control and processing capabilities.

Virtex-II Pro Details

The Virtex-II Pro devices offer the highest performance signal processing solution available. Each device contains a high density array of embedded multipliers (up to 556) and multiple on-chip memory banks that enable high-speed vector processing. An extensive library of intellectual property is available for the Virtex-II Pro devices. These FPGAs allow Gigabit connectivity for high-bandwidth, low-latency FPGA communication. System level design tools are available, such as *System Generator for DSP*, that bridge the gap between FPGA implementation and DSP system-level design. Table 1 below highlights the Virtex-II Pro capabilities used on the CHAMP-FX.

Table 1: Virtex-II Pro Features

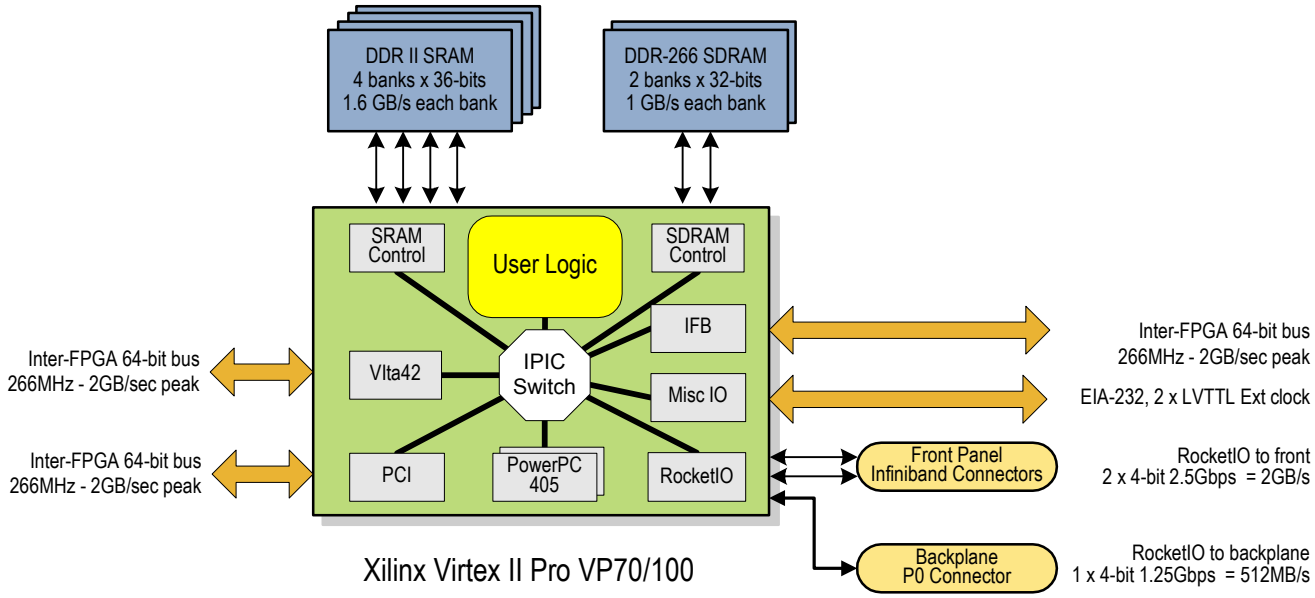
Device	PowerPC Blocks	Logic Cells	Slices	Flip-Flops	Multiplier Blocks	Block RAM (Kbits)
XC2VP70	2	74,448	33,088	66,176	328	5,904
XC2VP100	2	99,216	44,096	88,192	444	7,992

User FPGA Architecture

Each user FPGA has a variety of external I/O and memory interfaces as shown in Figure 2. Some or all of the following interfaces may be implemented in a user FPGA design:

- Up to four 36-bit DDR II SRAM interfaces
- Up to two 32-bit DDR SDRAM interfaces
- Up to four off-board, 4-bit RocketIO interfaces
- 66 MHz/64-bit PCI interface
- VITA 42.3 (XMC) mezzanine interface
- 64-bit inter-FPGA bus interface

Figure 2: User FPGA Block Diagram



DDR SDRAM

Each FPGA node interfaces to two 32-bit banks of 128 Mbyte, Double Data Rate (DDR) SDRAM. The instantaneous peak data transfer rate to each DDR SDRAM is 1 GB/s at 132 MHz. The SDRAM interface may be implemented as two independent 32-bit interfaces or a single 64-bit interface. The SDRAM is intended for temporary data storage, historical data storage and as a scroll buffer. The SDRAM may be implemented as an addressable RAM, a generic FIFO interface or a circular data buffer.

DDR II SRAM

Each FPGA node interfaces to four 2 Mbyte, 36-bit banks of DDR II SRAM for a total of 16 Mbytes (18 Mbytes if using 9th bit). The instantaneous peak data transfer rate to each DDR II SRAM is 1.6 GB/s at 200 MHz. The SRAM interface may be implemented as four independent 36-bit interfaces, two 72-bit interfaces or a single 144-bit interface. The SRAM is intended for temporary data storage associated with DSP algorithms like FFTs or filters. The SRAM may be implemented as an addressable RAM or a generic FIFO interface.

FPGA Internal Memory

The Virtex-II Pro has an unprecedented amount of internal FPGA memory resources as shown in Table 1. The FPGA contains hundreds of 18 Kbit Select RAM block memories. Each Select RAM block is a true 18 Kbit dual-port RAM with independent clocking on each port. These memories can be easily configured as single-port, dual-port, or FIFO memory structures and are instrumental in achieving high performance in DSP applications.

Inter-FPGA Bus

The Inter-FPGA bus is intended for high-bandwidth communications between the two user FPGAs. The bus is structured as an 64-bit, 2.5V LVCMOS or LVDS, generic interface including clock and control signals. It allows a flexible, high-performance, user-defined interface between FPGAs. Operational speeds up to 132 MHz are achievable, resulting in a 1.1 GB/s communication pipe between FPGAs.

Mezzanines

PMC Support

The CHAMP-FX is equipped with two PMC/XMC sites supporting 64-bit, 66 MHz PCI transfers. The board is backward compatible with either 32-bit or 64-bit PMCs at 33 or 66 MHz allowing peak data transfer rates up to 528 MB/s. The CHAMP-FX may only accept 3.3V or universal signaling PMC cards and is not 5.0V tolerant. The conduction-cooled versions of the CHAMP-FX adhere to the ANSI/VITA 20-2001 standard for conduction-cooled PMCs. The CHAMP-FX thermal frame provides the best possible thermal interface for PMC modules by supporting the primary and secondary thermal interfaces as defined by ANSI/VITA 20-2001. The thermal frame supports a mid-plane thermal shunt.

Processor PMC

The CHAMP-FX PMC sites are capable of hosting non-monarch processor PMCs (PrPMC) as defined in VITA 32-2003. The on-board *Configurator* FPGA performs PCI bus initialization, discovery and enumeration. The CHAMP-FX does not support Monarch PrPMC cards, but handles PCI central functions and interrupt control through the *Configurator* FPGA.

XMC (VITA 42)

The CHAMP-FX is also designed to accommodate two VITA 42 compliant XMC (Switched Mezzanine) cards. An XMC module is equipped with additional connectors to support a high-speed serial interface. The CHAMP-FX implements a 4-bit, bi-directional RocketIO interface to the XMC connector. This interface can support either of the two VITA 42 standards that define PCI Express (VITA 42.3) or Serial RapidIO (VITA 42.2) protocols, or it can be adapted to custom protocols if desired. At 2.5Gbps, the interface provides a bi-directional bandwidth of 2Gbytes/s. Contact the factory for specific interface protocol support.

Off-Board I/O

StarFabric Interface

The CHAMP-FX includes two independent off-board StarFabric interfaces. Each Stargen SG2010 PCI-StarFabric bridge is connected to a 66 MHz/64-bit PCI bus. Sustained data rates of 440 MB/s may be realized on the StarFabric using bundled links. The fabric interface allows system connectivity to our single board computers and DSP processing cards such as the CHAMP-AV product family. PCI DMA controllers are provided as IP to allow FPGA data movement to and from the PCI bus.

RocketIO and VITA 41 (VXS) interfaces

Xilinx RocketIO is supported on the CHAMP-FX. The RocketIO transceivers allow a variety of serial interconnect technologies to be used for off-board connectivity such as Xilinx Aurora, PCI express or serial RapidIO. Configured as bi-directional, 4-bit (four differential pair) links, these paths provide low latency, high performance FPGA or sensor interconnects.

For backplane connections, the CHAMP-FX is fitted with a VITA-41 (VXS) compatible high-speed P0 connector. Two 4-bit interfaces, one per FPGA, are present on the P0 connector. Rear panel links may operate up to 3.125Gbps. (bi-directional bandwidth 2.5Gbytes/s). The CHAMP-FX may be used in a standard VITA-41 backplane in conjunction with switch cards that support PCIe or Serial RapidIO. (Consult factory for specific protocol support). Backplanes are also available that support P0-P0 mesh architectures that are appropriate for developing custom sensor to CHAMP-FX applications. For compatibility with 95-pin P0 equipped VME64x backplanes, the CHAMP-FX may be ordered without the VITA41 connector.

The CHAMP-FX also provides two 4-bit RocketIO ports (one per FPGA) to the front panel via InfiniBand-style MicroGigaCN connectors. The front panel connectors are populated in the “keep-out” area of the PMC The choice of PMC or front-panel connectors is an order option.

PMC I/O

32 bits of PMC I/O is routed from each PMC Pn4 connector to the VME P0 and P2 connectors. This allows rear panel I/O connectivity for PMC/XMC modules. In the P0 case, this is an optional configuration making use of pins deemed reserved by the VITA 41 specification.

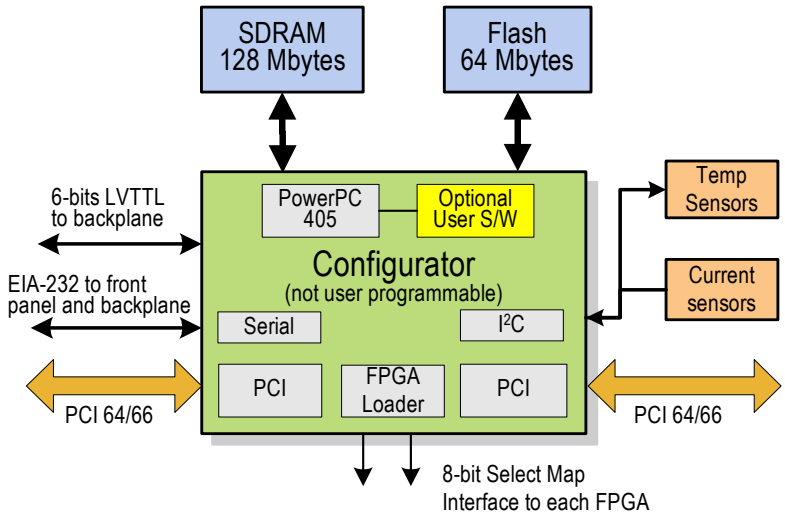
Configurator

The *Configurator* is an FPGA-based resource on the CHAMP-FX that manages PCI initialization, discovery and enumeration, board interrupt control, FPGA configuration file management, a serial port and thermal/power management. The *Configurator* functionality is contained in a separate Virtex-II Pro FPGA and takes advantage of the internal 405 PowerPC. The *Configurator* is automatically loaded from a serial EPROM upon reset.

Architecture

The *Configurator* FPGA is based on a Virtex-II Pro device (XC2VP20) that interfaces to two PCI buses, SDRAM and Flash memories, a serial debug port and I^2C power management devices. The architecture of the *Configurator* is shown in Figure 3.

Figure 3: Configurator Block Diagram



Embedded Processor

The *Configurator* makes use of the internal IBM 405 PowerPC. The *Configurator* is responsible for initializing and managing the CHAMP-FX on-board resources. The 405 PowerPC operates at 264 MHz and uses internal block RAM for boot-up code storage and cache memories. The external Flash may also be used for code storage for user applications.

Flash Memory

The Flash memory is accessible by the *Configurator* FPGA and contains multiple FPGA user configuration files, Built-In Test (BIT) FPGA configuration files and PowerPC application code. The 64 Mbyte Flash memory is 32-bit wide and is accessible in 32-bit increments from the *Configurator* or either PCI interface. The Flash memory is large enough to hold multiple FPGA configuration files. A write protection jumper is also provided to disable Flash memory writes for security purposes.

SDRAM

The *Configurator* also has an external 128 Mbyte SDRAM for PowerPC code execution and volatile storage of FPGA configuration files. This feature is useful for fast FPGA reconfiguration and storage of classified data or algorithms. The memory is accesible from the *Configurator* as well as either PCI bus.

Flash File Management

The *Configurator* FPGA is initialized from a serial EPROM that may be updated through the JTAG programming interface. The *Configurator* is responsible for loading configuration files for the User FPGAs. The configurator loads configuration files from Flash or SDRAM depending upon Flash configuration parameters. The user FPGAs may be configured individually or simultaneously, depending on the user command through the 8-bit SelectMap interface. The following table shows the SelectMap configuration times for three FPGA devices.

Table 2: User FPGA Configuration Times

Device	Configuration File Size (bits)	Configuration Time from Flash (ms)	Configuration Time from SDRAM (ms)
XC2VP70	26,099,040	TBD	65
XC2VP100	34,292,832	TBD	85

Thermal Management

The CHAMP-FX contains temperature sensors that monitor the card temperature. Thermal management is key when dealing with large FPGAs that can consume a significant amount of power. The *Configurator* monitors the sensors through an I^2C bus. The thermal sensors provide a programmable over-temp status that is used to illuminate a red LED as well as provide an interrupt to the system. The software API allows the user to poll the card and die temperatures during development and deployment.

Power Management

The *Configurator* provides current monitoring circuitry to report each FPGA's power consumption. The *Configurator* interfaces to the power management circuitry through the I^2C bus. The software API enables the user to monitor the individual FPGA power consumption.

General Purpose I/O

The CHAMP-FX provides six general purpose LVTTL I/O lines which are accessible at the P2 connector. The GPIO signals may be configured individually to be input or output, and separately configured to be open drain or LVTTL. These pins are controlled by the *Configurator FPGA* and may be defined as interrupts.

Miscellaneous

Serial Ports

The CHAMP-FX provides three serial ports. One port from the *Configurator* is used for an EIA-232 debug port. This port is controlled by the 405 PowerPC within the *Configurator*. The SW API uses this port for command, control and status information for the CHAMP-FX. A single EIA-232 port is also available in each user FPGA for user defined functionality. The serial ports may operate at up to 56 Kbaud. The *Configurator* serial port is routed to the front panel, while the other user FPGA serial ports are routed to the rear panel P2 connector.

Indicator LEDs

The CHAMP-FX provides twelve user-controllable, green LEDs. Six of these are visible on the front panel of the air-cooled versions and six more are located on the back of the board. Each user FPGA has control over two LEDs on the front panel and two on the back of the card. There is an additional red LED on the front panel used to indicate a failure determined by the on-board *Configurator* diagnostic firmware. There are two red LEDs mounted on the back of the card to indicate an over-temperature condition on the FPGA. There are also two green LEDs on the back of the card to indicate valid StarFabric link status.

CHAMPTools-FX

The *CHAMPTools-FX* library includes the following functionality:

- CHAMP-FX Hardware and Software User's Manuals
- CWCEC VHDL IP library
- User FPGA infrastructure
- Example reference designs
- *Configurator* software library
- VHDL simulation testbench
- Support for Xilinx ISE and ChipScope Pro tools

Refer to the *CHAMPTools-FX* datasheet for more details.

Options

The following configuration options are planned:

- FPGA options: XC2VP70 or XC2VP100 devices
- Front panel Rocket I/O connectors
- Depopulation of P0 connector

Contact the factory for other configurations options including higher density memory for Flash, DDR SDRAM and DDR II SRAM memories.

Specifications

The CHAMP-FX is available in a full range of environmental grades starting from commercial air-cooled to extended temperature, rugged, conduction-cooled versions. This allows the customer to select the board to match the environmental requirements of the platform.

The tables below show the power, dimensions and weight of the card.

Table 3: Power Requirements

Power Requirements (without PMCs)	
5.0V	TBD
3.3V	TBD
+12V	Only used for PMC power
-12V	Only used for PMC power

Table 4: Dimensions and Weight

Dimensions and Weight		
Option	**Dimension**	**Weight**
Air-cooled	Per ANSI/VITA 1-1994	650 grams (1.43 lbs)
Conduction-cooled	Per IEEE 1101.2-1992	928 grams (12.04 lbs)

Note: Air-cooled cards available in level 0 and level 100.

Note: Conduction-cooled cards available in level 100 and level 200.*

* Refer to Ruggedization Guidelines data sheet for more information.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales or

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com