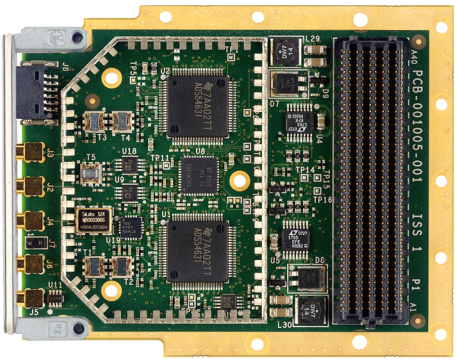
Data Sheet

ADC510

Dual-Channel 500/550 MSPS Analog Input FMC



Applications

- Signal Intelligence (SIGINT)
- Electronic Counter Measures (ECM)
- Radar

Features

- Dual 500/550 MSPS 12-bit ADCs
- 1.5 GHz input bandwidth
- Onboard sample clock
- External clock input
- FMC/VITA 57 form factor
- Air- or conduction-cooled rugged versions

Benefits

- Direct ADC connection to host FPGA ensures maximum throughput
- Able to synchronize multiple channels/boards
- Easily interfaces to FPGA-based host board
- Complete ADC I/O

Overview

The ADC510 is a dual-channel 500/550 MSPS analog input FPGA Mezzanine Card (FMC) based on the VITA 57 specification. This specification allows I/O devices to be directly coupled to a host FPGA. On the ADC510, the two ADC devices connect through the FMC site to an FPGA-based host board, maximizing data throughput and minimizing latency.

The ADC510 supports a choice of onboard sample clock frequencies as well as an external reference input. Multiple boards can be synchronized to increase the number of input channels. The ADC510 can be used on platforms like Curtiss-Wright Controls Embedded Computing's FPE650, a 6U quad Xilinx® Virtex®-5 FPGA VPX processor board.

Analog Input

Two analog inputs are supported through 50Ω MMCX type front panel connectors. The analog inputs are single-ended and are coupled to the ADCs using a balun and AC coupling capacitor configuration, in order to produce the broadband differential input required by the devices. The analog signal paths of both ADC inputs are matched to within 4ps to allow synchronous operation of the ADCs. The "Full Scale" analog input voltage is 2.2 Vpp (+11 dBm) at 1.5 GHz.

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Clocks, Triggers & Synchronization

An onboard oscillator is provided. The frequency can be selected by the carrier FPGA (through the FMC connector) for sample rates of 300, 320, 400 and 500 MSPS.

The external front panel clock input is through a 50Ω MMCX type front panel connector. The clock input is designed to operate at a typical frequency of 1.0 GHz but may operate at clock frequencies between 100 MHz and 1.1 GHz. The clock input may be sinusoidal or square, and is designed to operate with an input level between -2.0 dBm and +4.0 dBm. The analog sampling clock is derived from every 2nd rising edge of the input clock. It can be sourced from the carrier FPGA as part of the multi-board synchronization process.

Trigger In and Trigger Out use MMCX type front panel connectors. Actual functionality of these signals is dependent on the HDL code in the FPGA of the host carrier card. Trigger In is a single-ended LVPECL input signal. The maximum operating frequency of this input is designed to be approximately 300 MHz. Trigger Out is a single-ended LVPECL output signal.

It is possible to synchronize the ADCs on multiple ADC510s using the Trigger In and Trigger Out signals. The ADC510 FusionXF HDK & SDK support this functionality.

The GPIO connector on the ADC510 is an ERNI dual row right-angle male connector, SMC Type B. Eight General Purpose Input/Output (GPIO) signals are split into four pairs, which are routed as loosely coupled pairs across the FMC.

FusionXF Software/HDL Support

Curtiss-Wright's FusionXF development kit includes software, HDL and utilities with examples and infrastructure for using the ADC510 on each supported host.

One of the core elements to the FusionXF development kit is a framework for adding new IP functionality or capabilities to the FPGA. It facilitates the inclusion of signal processing blocks such as digital down converters, making HDL development easier and integration more straightforward.

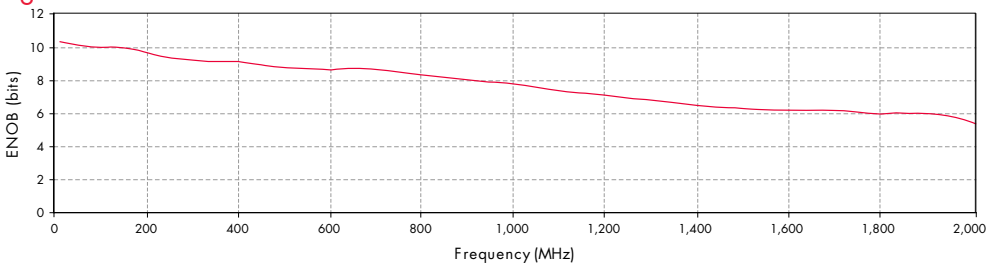
Analog Performance

The following figures provide data from Curtiss-Wright's preliminary analog characterization of the ADC510. They represent typical measured performance.

Effective Number of Bits (ENOB)

The ENOB is above 9-bits in the first Nyquist region. The board characteristics correlate to those of the ADC device over the frequency range shown.

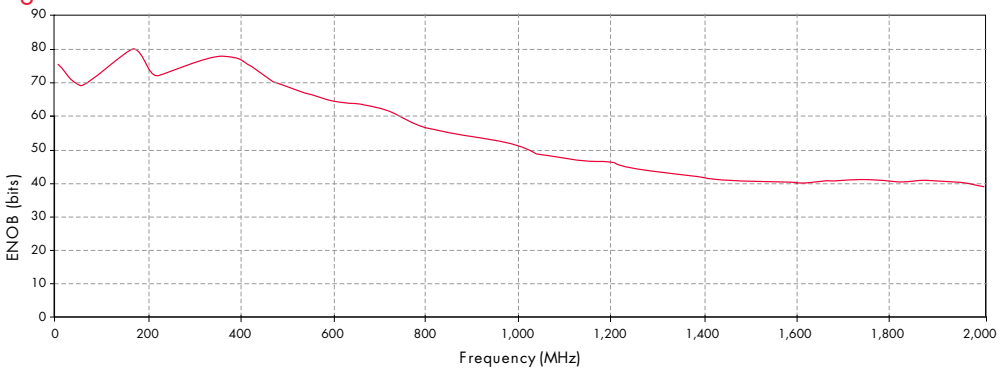
Figure 1: ADC510 ENOB



Spurious-Free Dynamic Range (SFDR)

The SFDR is shown below. The main non-linear element in the ADC510 is the balun which performs the broadband single-ended to differential signal conversion required for input to the ADC chip.

Figure 2: ADC510 SFDR



Signal-to-Noise Ration (SNR)

The SNR correlates well to the ADC device.

Figure 3: ADC510 SNR

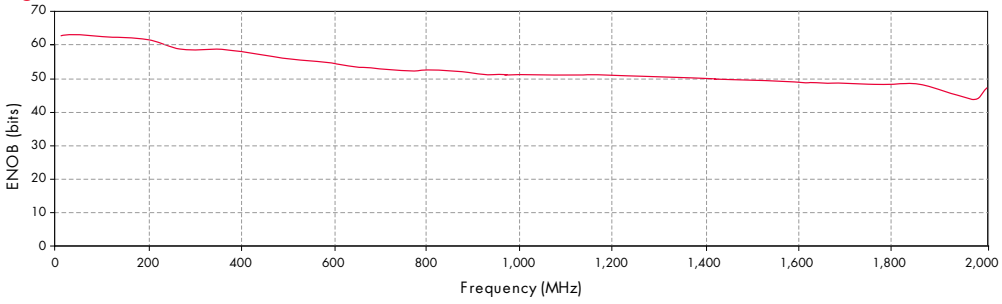




Table 1: Board Specifications

Analog Input	
Number of Channels	2, single-ended
Sampling Frequency	Up to 500 MSPS (550 MSPS with ADS54RF63)
Full Scale Input Voltage	2V2 pk-pk
Device	2x TI ADS5463 (or ADS54RF63)
Input Bandwidth (3dB)	1.5 GHz
Input Impedance	50 Ohm, AC coupled
SNR	58.94 @ 259 MHz
SFDR	74.43 @ 259 MHz
ENOB	9.47 @ 259 MHz
Clock & Trigger Inputs	
Clock Input Connector	Front panel MMCX
Clock Input	50 Ohm, AC coupled LVPECL -2.0 to +4.0 dBm input level (sine or square)
Clock Input Frequency	Sample rate is half input clock frequency (i.e. 1 GHz for 500 MSPS)
Internal Clock	Selectable from: ◆ 600 MHz: 300 MSPS ◆ 640 MHz: 320 MSPS ◆ 800 MHz: 400 MSPS ◆ 1000 MHz: 500 MSPS
Trigger Input/Output	Single-ended, 50 Ohm, LVPECL buffered to host FPGA

Misc.	
LEDs	2x yellow (host FPGA controlled)
Digital I/O	4 differential pairs
Power Supplies	
12 V (+/- 5%)	700 mA
3.3 V (+/- 5%)	200 mA
3.3 V Aux (+/- 5%)	5 mA
VADJ	2.5 V (+/- 5%) 250 mA
Software/HDL Code	
Host HDL Code	FusionXF HDL support (contact Curtiss-Wright for supported hosts)
Environmental	
Ruggedization Levels	◆ Air-cooled ◆ Air-cooled rugged ◆ Conduction-cooled RoHS compliant (contact factory for leaded builds)

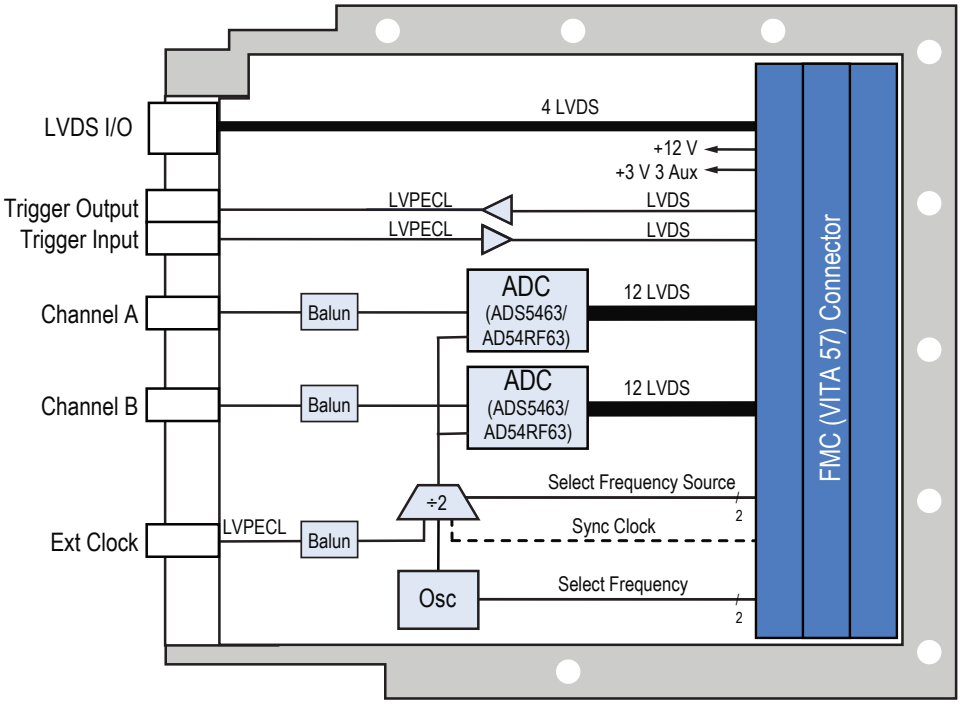
Note:
All the analog characterizations in this datasheet represent the measured performance of a standard production board in normal laboratory conditions. These are typical performance figures and are not guaranteed.

Table 2: Environment Specifications

		Air-cooled			Conduction-cooled	
Part number extension		Level 0	Level 100	Level 200 (Note 6)	Level 100	Level 200
Temperature	Operational (Air-cooled Note 4) (Conduction-cooled Note 7)	0 to +50 °C	-40 to +71 °C	-40 to +85 °C	-40 to +71 °C	-40 to +85 °C
	Non-operational (storage)	-40 to +85 °C	-55 to +125 °C	-55 to +125 °C	-55 to +125 °C	-55 to +125 °C
Vibration	Sine (Note 1)	2g peak 15-2k Hz	10g peak 15-2k Hz	10g peak 15-2k Hz	10g peak 15-2k Hz	10g peak 15-2k Hz
	Random (Note 2)	$0.01g^2$/Hz 15-2k Hz	$0.04g^2$/Hz 15-2k Hz	$0.04g^2$/Hz 15-2k Hz	$0.1g^2$/Hz 15-2k Hz	$0.1g^2$/Hz 15-2k Hz
Shock (Note 3)	Operational	20g peak	30g peak	30g peak	40g peak	40g peak
Humidity	Operational	0-95% non-condensing	0-100% non-condensing	0-100% non-condensing	0-100% non-condensing	0-100% non-condensing
	Non-operational (storage)	0-95% non-condensing	0-100% condensing	0-100% condensing	0-100% condensing	0-100% condensing
Conformal Coat (Note 5)		No	Yes	Yes	Yes	Yes

Notes:
1. Sine vibration based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15-44 Hz, depending on specific test equipment.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Standard air-flow is 8 cfm at sea level. Some higher-powered products may require additional airflow. Consult the factory for details.
5. Conformal coating type is manufacturing site-specific. Consult the factory for details.
6. This is a non-standard product. Consult factory for availability.
7. Temperature is measured at the card edge.

Figure 4: ADC510 Block Diagram



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

Technical Support

For technical support:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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