VPX3-673A

CMOSS/SOSA 3U VPX Assured Position, Navigation, and Timing (A-PNT) Solution

The VPX3-673A from Curtiss-Wright Defense Solutions is a rugged, high performance 3U OpenVPX™ A-PNT solution and Central Radial Clock module. With a quad-core Arm® A53 processor, a dual-core R5 real-time processor, and the programmable logic (PL) sections, the Xilinx® MPSoC controls the board and handles the algorithm processing. Aligned with the Open Group Sensor Open Systems Architecture™ (SOSA) radial clock profile SLT3x-TIM-2S1U22S1U2U1H-14.9.2-1, this card supports the VICTORY prototcol as well as CMOSS requirements.

The VPX3-673A serves as an excellent high-performance, low-skew clock master powered by a GPS-disciplined low noise Chip Scale Atomic Clock (LN-CSAC). The VPX3-673A also supports a configuration option for the LN-CSAC to function in free-running mode. The VPX3-673A has the option to act as an NTP master or slave, as well as the ability to be an IEEE-1588 v2 (PTP) grand master.

With an on-board 10 degree of freedom inertial measurement unit (IMU), the VPX3-673A is capable of precise motion tracking in a denied or untrusted GPS environment.

The VPX3-673A 1PPS source is user selectable from multiple options including GPS, Alternative RF Navigation, onboard LN-CSAC or backplane Ethernet connections on P0, P1, or P2. External REF and AUX clock sources can be brought in via a P0 bused clock, or a P1 or a P2 radial clock. Synchronized radial clock outputs are available on P0 (bused clock), P1(11 outputs), and the P2 VITA 67.3 coax. Output REF and AUX clocks can be dynamically shifted in software allowing the VPX3-673A to compensate for backplane trace length differences.

Multiple VPX3-673As can be synced together using the COAX_CLK1 signals (in and out) configured as embedded PPS (ePPS) signals.

The VPX3-673A supports an internal GPS module, or an external GPS via an easily accessible front panel connector. The onboard GB-GRAM Type II GPS Receiver supports SAASM, M-Code, including dedicated zeroize and key fill functionality.

The VPX3-673A has an integrated Alternative RF Navigation receiver. Alternative RF Navigation is a space-based commercial system that is being evaluated by the Army as alternative source of position, navigation, and timing (PNT) information on the battlefield. Army requirements for alternative and complementary PNT capabilities continue to be developed and refined in coordination with the Army's joint partners, the Department of Homeland Security, and others.

Key features

- Provides a high-assurance accurate navigation and timing solutions in GPS denied environment
- Acts as system wide timing master by providing reliable clock signals
- Provides Atomic clock backed NTP/PTP timing for distributed network use
- Aligns with the SOSA Technical Standard to meet the 3U Radial Clock (timing) profile
- Supports standard M-Code and SAASM GPS modules
- Outputs: 11 Radial clock pairs of 10-125 MHZ 1PPS aligned
- Supports external PNT sources over Ethernet
- Ability to sync multiple VPX3-673As
- A-PNT Software US Only Version
- **pntOS**
- **Alternative RF Navigation**
- VICTORY

Applications

- Assured PNT
- Radial Clock Distribution

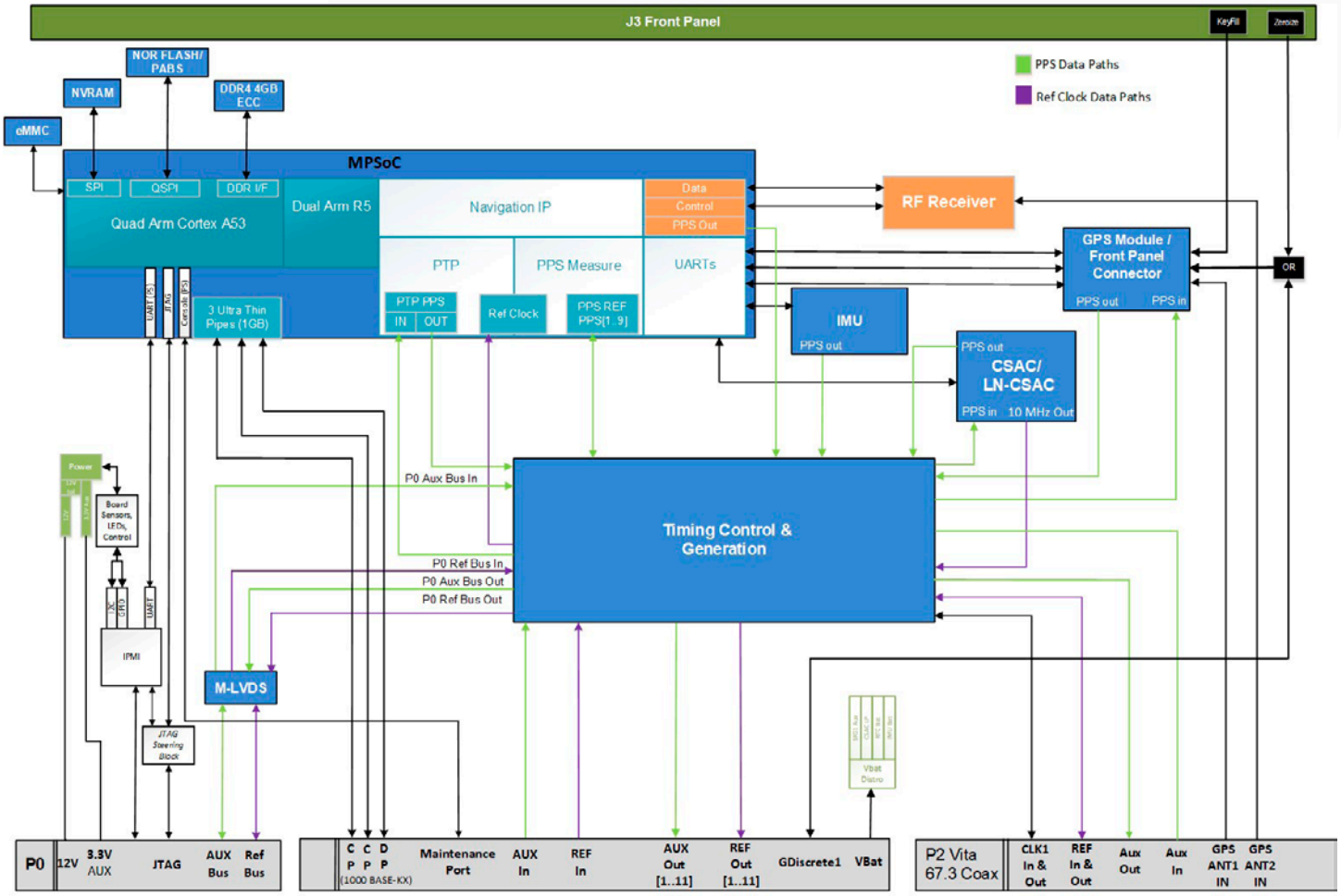

Figure 1: VPX3-673A block diagram

In addition to Alternative RF Navigation, the VPX3-673A also includes pntOS software. As an open source, government-owned plug-in architecture for building integrated PNT sensor-fusion applications, pntOS significantly reduces the time and effort required to develop algorithms and add support for new sensors.

The VPX3-673A also supports Intelligent Platform Management Interface (IPMI), JTAG, and a backplane maintenance port to provide a serial console.

Based on Curtiss-Wright's Common A-PNT Software Load® (CSAL®), the software options for the VPX3-673A include full-featured A-PNT software, as well as software development kits (SDK)s for the United States and the rest of the world. The A-PNT sensor fusion software uses data from multiple sensors to maintain PNT in GPS-denied environments. These algorithms are powered by pntOS which combines and arbitrates the disparate but complementary sensor data. A fully government-owned open architecture for PNT, pntOS defines and standardizes the interfaces to PNT system components with modular plugins. By design, external sensors can be added to enhance the accuracy and durability of the A-PNT-fused solution.

For customers that want to develop/deploy their own A-PNT or timing algorithms, the VPX3-673A SDK provides the tools and the hardware drivers to build their own applications. Please refer to the DSW-673A-SDK datasheet for more details.

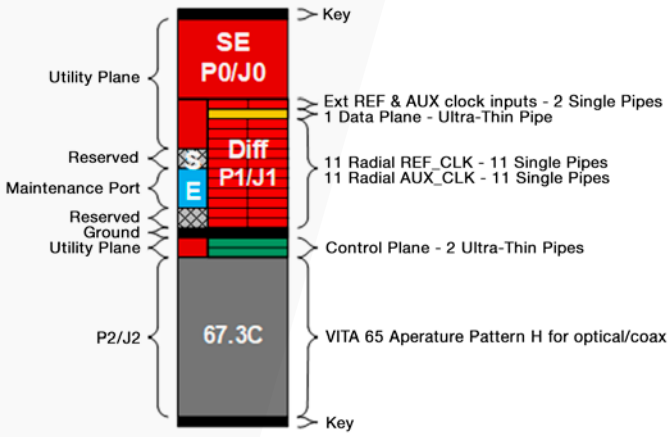

Figure 2: SLT3x-TIM-2S1U22S1U2U1H-14.9.2-1

Specifications

Form factor

- 3U OpenVPX, developed in alignment with the SOSA* Technical radial clock profile
  - + SLT3x-TIM-2S1U22S1U2U1H-14.9.2-1
  - + MOD3-TIM-2S1U22S1U2U1H-16.9.2-1

** per SOSA Reference Architecture Edition 1.0, Version 3 dated May 2020*

PPS Source Options

- GPS (internal or external)
- Alternative RF Navigation
- P0 Bus Clock Aux
- P1 Radial Clock Aux In
- P2 COAX Clock Aux In (B1)

Ref Clock Source Options

- LN-CSAC 10 MHz
- P0 Bus Clock Ref
- P1 Radial Clock Ref In
- P2 COAX Ref In (B2)

A-PNT Features

- Low Noise Chip-Scale Atomic Clock (LN-CSAC)
  - + Low noise
  - + High stability
- Inertial Measurement Unit (IMU)
  - + 10 degrees of freedom
  - + 3-axis accelerometers
  - + 3-axis gyros
  - + 3-axis magnetometers
  - + Barometric pressure sensor

Weight

- Estimate Weight with GPS, and covers supporting two level maintenance handling: 625g

Power

- Maximum power consumption = 36.2 watts (estimated)
- 12 VDC Primary power, 3.3V Aux Power

Front I/O

- Front Panel Connector (for external GPS)
- Key fill
- Zeroize

Rear I/O Timing

- P0
  - + Bused clock
- P1
  - + Output: 11 x radial clocks
  - + Input: 1 x radial clock
- P2 (Vita 67.3 COAX)
  - + Ref clock in and out
  - + Aux clock in and out
  - + CLK1 in and out
  - + 1 GPS antenna in
  - + 1 GNSS antenna in

Backplane Ethernet ports

- 2 x 1000 BASE-KX control planes
- 1 x 1000 Base-KX data plane

MPSoC Based Processing System

- Quad-core ARM A53 processor @ 1.2 GHz
- Dual-Core R5 Real time Processor
- 4 Mb mRAM
- 2 GB NOR Flash/PABS
- 16 GB eMMC
- 4GB DDR4
- IPMI control
- JTAG
- RS-232 to backplane for console (LVCMOS maintenance port)

CASL & pntOS Software Support

- A-PNT sensor fusion solution
- VICTORY message format support
- User defined plugin compatibility for external sensors
- Secure boot, signed application

Environmental

- VITA 48.2 1” Conduction-cooled
  - + Operational: -20 to +60° C
  - + Storage: -40 to +85° C

Rear Transition Module

For building systems in the lab environment, Curtiss-Wright provides a Rear Transition Module which plugs into the backside of the VPX3-673A’s backplane and provides access to many of the board I/O interfaces on industry standard connectors.

Table 1 P2/67.3 COAX (10-pin connector)

	1	2	3	4
A	REF_CLK_OUT	AUX_CLK_OUT	CLK1_OUT	
B	AUX_CLK_IN	REF_CLK_IN	CLK1_IN	Not Used
C	Not Used	ALT_NAV_IN	GPS_ANT_IN	

Table 2 P0 Clocks

SIGNAL	FREQUENCY		LEVELS	TYPICAL USE CASE
	MIN	MAX		
BUSED REF_CLK	10 MHz	125 MHz	M-LVDS	100 MHz
BUSED AUX_CLK	---	---	M-LVDS	1 PPS

Table 3 P1 Clocks

SIGNAL	FREQUENCY		LEVELS	TYPICAL USE CASE
	MIN	MAX		
REF_CLK IN	10 MHz	125 MHz	LVDS	100 MHz
AUX_CLK IN	---	---	LVDS	1 PPS
REF_CLK OUT [1..11]	10 MHz	125 MHz	LVDS	100 MHz
AUX_CLK OUT [1..11]	---	---	LVDS	1 PPS

Table 4 P2 Clocks Vita 67.3

SIGNAL (50 Ω CABLE DRIVER)	FREQUENCY		TYPICAL USE CASE
	MIN	MAX	
REF_CLK IN	10 MHz	125 MHz	100 MHz
AUX_CLK IN	---	---	1 PPS
CLK1 IN	10 MHz	25 MHz	ePPS – sync multiple 673A
REF_CLK OUT	10 MHz	125 MHz	100 MHz
AUX_CLK OUT	---	---	1 PPS
CLK1 OUT	10 MHz	25 MHz	ePPS – sync multiple 673A

VPX3-673A ordering information

To order the VPX3-673A product or software services, contact your local Curtiss-Wright sales representative or email ds@curtisswright.com.

PART NUMBER	DESCRIPTION
VPX3-673A-C10AA-E	EAU 3U VPX SOSA A-PNT card
RTM3-673A-0000	Extended 3U Rear Transition Module for the development environment to access key backplane signals
DSW-673A-SDK-000	Drivers & tools to develop A-PNT or timing algorithms (US Version)
DSW-673A-SDK-001	Drivers & tools to develop A-PNT or timing algorithms (Open version)
MNT-673A-SDK-000	Annual support & maintenance for DSW-673A-SDK-000
MNT-673A-SDK-001	Annual support & maintenance for DSW-673A-SDK-001

Note: Please contact Curtiss-Wright Defense Solutions for features supported in the EAU.