VPX3-673

3U VPX™ Assured Position Navigation and Timing (A-PNT)

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Key Features

- NXP® QorIQ Layerscape LS1043A Quad Core v8 64-bit Arm A53 at 1.6 GHz
- 2 or 4 GB DDR4 at 1600 MT/s with ECC
- Up to 16 GB eMMC flash
- GPS GB-GRAM Type II connector
- Chip Scale Atomic Clock (CSAC)
- On-board 10 Degree of freedom Inertial Measurement Unit (IMU)
- VITA 67.3C (RF) P2 connectors
- Differential radial clock driving slot profile on P1 connector
- Support for external RS-422 and RS-232
- Available in air-cooled and conduction-cooled versions
- Supports Linux® TBD

Applications

- Assured PNT
- Radial Clock Distribution

Overview

The VPX3-673 from Curtiss-Wright Defense Solutions is a rugged, high-performance 3U OpenVPX™ A-PNT solution and Central Radial Clock module. It features a Single Board Computer (SBC) that combines NXP's capable and low-powered QorIQ® Layerscape LS1043A Quad Core 64-bit v8 Arm® A53 with a full suite of supporting capabilities on-board to enable A-PNT processing and distribution. The VPX3-673 supports CMOSS & SOSA Timing Module requirements.

The VPX3-673 supports NXP's Arm processor technology, featuring its Layerscape LS1043A. Utilizing this advanced 64-bit, 4-core CPU and Curtiss-Wright's proven ruggedization technology, the VPX3-673 has been designed for harsh environments, making it ideal for architecting high-performance computing and processing systems for A-PNT.

With a high speed DDR4 memory subsystem connected directly to the processor and supporting up to 4 GB SDRAM, the VPX3-673 is able to maximize the performance of the multiple processing cores, GPS, and associated position and timing capabilities.

The VPX3-673 serves an excellent high-performance, low-skew clock master powered by a GPS-disciplined Chip Scale Atomic Clock (CSAC), which offers a variety of configurable clock reference sources and support for up to 16 synchronized clock outputs.

With an on-board 10 degree of freedom inertial measurement unit (IMU), the VPX3-673 is capable of precise motion tracking in a denied or untrusted GPS environment. Support for an on-board GPS Receiver (SAASM GB-GRAM Type II, upgradeable to M-Code) is provided, including dedicated zeroize and keyfill functionality. An RS-232 port and an RF 1 PPS input provides an interface for external RS-232 GPS sources. Interfaces for external, high-performance Inertial Navigation Systems and Measurement Units are provided.

For Control Plane connectivity, the VPX3-673 supports two high-speed Ethernet fabric ports at 1000Base-KX and 10G-BASE-KR, with an option for Fast Ethernet Controller (FEC) respectively.

The VPX3-673 provides a suite of software support targeted to a Linux operating system environment.

SOSA™ Sensor Open Systems Architecture MEMBER

arm

OpenVPX™

VPX REDI™

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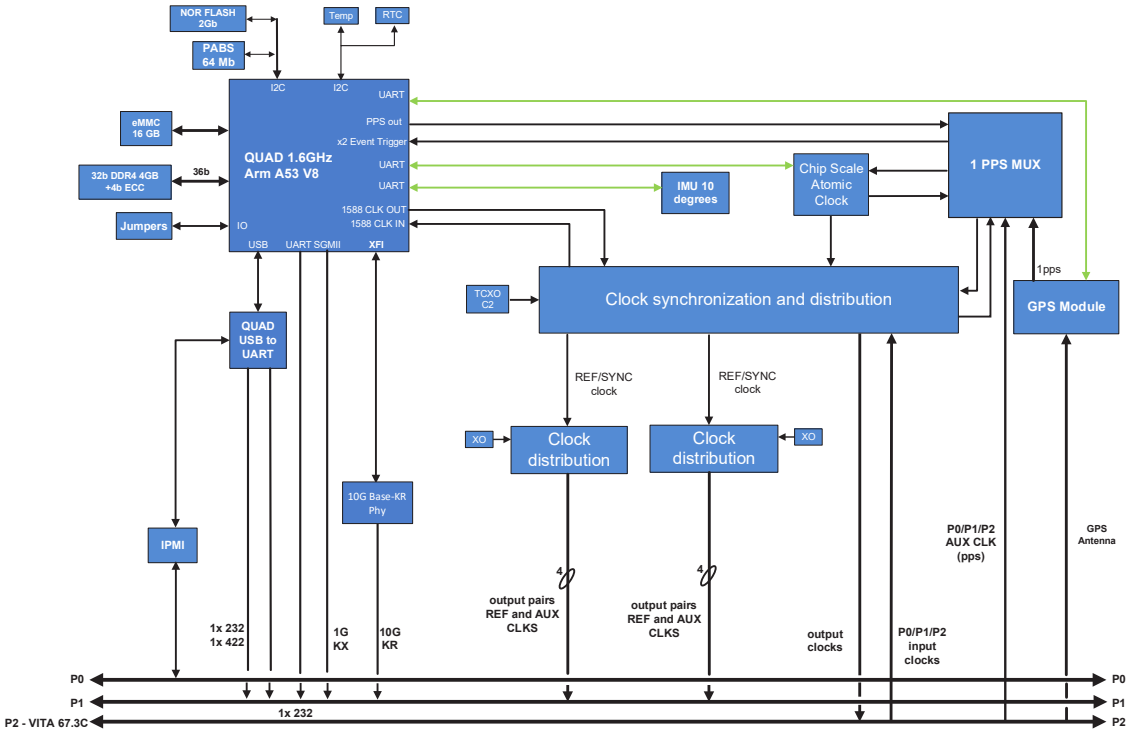

Figure 1: VPX3-673 block diagram

Features Summary

Form factor

- 3U OpenVPX, supporting radial clock driving slot profile SLT3x-TIM-4S16S1U2U1H-14.9.1-1

Processor

NXP LayerScape LS1043A processor

- 4-Core @ 1.6 GHz (64-bit)
- 32 kB L1 I/D cache per core, 1 MB shared L2 cache
- Neon SIMD co-processor
- Arm v8 cryptography extensions
- IEEE-754 complaint VFPv4 floating point
- DPAA parse, classify and distribution
- Arm SMMU for hardware enhanced virtualization
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification and distribution (FMan)
  - Queue management for scheduling, packet sequencing and congestion management (QMan)
  - Hardware buffer management for buffer allocation and de-allocation (BMan)
  - Cryptography acceleration (SEC)

SDRAM memory

- Up to 4 GB 32-bit DDR4 at 1600 MT/s with ECC

Non-volatile memory

- Up to 64 GB eMMC flash
- 2 Gb QSPI flash for boot functions

Backplane fabrics/Ethernet ports

- 1 x 10G Ethernet port – SerDes KX/KR
- 1 x 1G Ethernet port – SerDes KX

Rear I/O

- 2 x RS-232 serial channels
- 1 x RS-422 serial channel
- Radial clocks - 8 x differential ref and aux
- RF timing (P2)
  - 1 x GPS antenna
  - Aux. in, out
  - Ref. in, out
  - Clk. in, out
- Backplane timing (P1)
  - 1 x Ref. in, 8 x out.
  - 1 x Aux in, 8 x out
  - 2 x User defined (TBD)
- JTAG
- IPMC Support

Security features

- Arm v8 cryptography extensions
- Cryptography acceleration unit (SEC)
- UEFI Secure Boot
- NXP Secure Boot and Trust Architecture
- Arm Trustzone®

Software support

- Linux (TBD)

Built-in Test (TBD)

VPX3-673 Features

NXP Arm A53 Quad-Core CPU

The NXP QorIQ LayerScape LS1043A processor is based on Arm's industry-leading silicon technology and the latest micro-architecture enhancements, adding additional value with 64-bit processing and extended virtual addresses. The LS1043A delivers high performance and unmatched low power levels critical to today's Size, Weight, and Power (SWaP) sensitive designs.

The LS1043A processor includes the following features:

- 4-Core @ 1.6 GHz (64-bit)
- 32 kB L1 I/D cache per core, 1 MB shared L2 cache
- Neon SIMD co-processor
- Arm v8 cryptography extensions
- IEEE-754 complaint VFPv4 floating point
- DPAA parse, classify and distribution
- Arm SMMU for hardware enhanced virtualization

Power consumption and CPU tuning

The LS1043A provides extremely flexible and dynamic methods of controlling power consumption. From statically parking cores in the OS to dynamically adjusting CPU clocks at run time, the LS1043A performance can be tailored to meet a wide range of processing and power requirements.

Dual Data Rate (DDR4) SDRAM

The VPX3-673 processor has a built-in 32-bit plus 4-bit ECC DDR4 memory controller. The VPX3-673 may be fitted with 2, or 4 GB of DDR4 SDRAM. The DDR4 interface operates at 1600 MT/s, yielding a raw memory throughput performance of 6.4 GB/s. The SDRAM is accessible from the processor as well as from the 1G/10G Ethernet control planes.

eMMC Flash

The VPX3-673 is configured with Non-Volatile embedded Multi-Media Controller (eMMC) local flash storage connected directly to the processor. The integration of the flash controller relieves the processor from having to perform low-level flash memory management.

Radial Clocks

The LS1043A provides a variety of clocking interconnect to the VPX Expansion Plane, used to receive and transmit clocking information in a synchronized system. The VPX3-673 accepts reference and auxiliary clock inputs, and sources eight synchronized reference and auxiliary clock outputs to the backplane and the front panel. The synchronization of the clocks are tunable to allow for backplane differences.

Common use of the reference and aux clocks is to provide a high-precision radial clock source to synchronize multiple cards in a system to a common reference clock, which is disciplined by the on-board CSAC.

TABLE 1 P1 Timing Sources and Clocks

SIGNAL	FREQUENCY		LEVELS	SWING	JITTER	TIMING ALIGNMENT
	MIN	MAX				
Ref_Clock_ Out_n (P1)	1 Hz	500 MHz	LVDS, LVPECL	› LVDS: 840 mV Peak to Peak with configurable Common mode, typical is 1.23V › Programmable mode: 600mV to 1800mV Peak to Peak in 200mV steps › LVPECL: 1640 mV Peak to Peak	Freq dependent, <1ps typical <0.5 ps	TBD. See note
AUX_Clock_ Out_n (P1)	1 Hz	500 Mhz	LVDS, LVPECL	› LVDS: 840 mV Peak to Peak with configurable Common mode, typical is 1.23V › Programmable mode: 600mV to 1800mV Peak to Peak in 200mV steps › LVPECL: 1640 mV Peak to Peak	Freq dependent, <1ps typical <0.5 ps	TBD. See note

Notes: Per-synthesizer phase adjustment: 1 ps resolution. Output duty cycle control. Output alignment and phase adjustment: Base on Synthesizer frequency.

TABLE 2	P0 Clock Input Sources				
SIGNAL	FREQUENCY		LEVELS	JITTER	Typical Use Case
	MIN	MAX			
Ref_Clock	1 Hz	125 MHz (TBC)	M-LVDS	TBD	10 MHz
AUX_Clock	1 Hz	10 MHz (TBC)	M-LVDS	TBD	1 PPS

TABLE 3	P1 Clock Input Sources				
SIGNAL	FREQUENCY		LEVELS	JITTER	Typical Use Case
	MIN	MAX			
Ref_RClock_in	1 Hz	500 MHz (TBC)	LVDS	TBD	10 MHz
Aux_RClock_in	1 Hz	10 MHz (TBC)	LVDS	TBD	1 PPS
UD_timing-IN1	TBD	TBD	LVDS	TBD	
UD_timing-IN1	TBD	TBD	LVDS	TBD	

TABLE 4	P2 Clock Input Sources VITA 67.3C					
SIGNAL	FREQUENCY		Levels	JITTER	Typical Use Case	Notes
	MIN	MAX				
REF_CLK IN	1 Hz	180 MHz	Single-ended PECL	TBD	10 MHz	50 Ohm cable driver
AUX_CLK IN	1 Hz	10 MHz (TBC)	0-5V TTL	TBD	1 PPS	50 Ohm cable driver
CLK1 IN	1 Hz	180 MHz	Single-ended PECL	TBD	10 MHz	50 Ohm cable driver

TABLE 5	P2 Clock Output Sources VITA 67.3C					
SIGNAL	FREQUENCY		Levels	JITTER	Typical Use Case	Notes
	MIN	MAX				
REF_CLK OUT	1 Hz	180 MHz	0-2.37V	TBD	10 MHz	50 Ohm cable driver
AUX_CLK OUT	1 Hz	10 MHz (TBC)	0-2.37V	TBD	1 PPS	50 Ohm cable driver
CLK1 OUT	1 Hz	180 MHz	0-2.37V	TBD	10 MHz	50 Ohm cable driver

The synchronization signals on the expansion plane are as follows:

- LVDS radial clocks (P1)
  - 8 x differential ref clocks
  - 8 x differential aux clocks
- RF timing (P2)
  - 1 x GPS antenna
  - Aux. in, out
  - Ref. in, out
  - Clk. in, out

Ethernet Control Plane

The VPX3-673 provides one 10GBase-KR Control Plane Ethernet port and one 1000BASE-KX Control Plane Ethernet port. The 10GBase-KR port can also support directly driving an optical transceiver.

Serial ports

The VPX3-673 provides two RS-232 and one RS-422 serial channels to the VPX backplane. One RS-232 serial port provides dedicated console access. The serial ports support asynchronous communications with baud rates, independently configurable from 300 to 115,200 kBaud.

Temperature sensors

The VPX3-673 provides temperature sensors to measure board and processor temperatures. There is a sensor at each edge of the card and sensors built into the IPMI and using discrete sensors. The card edge sensors can be read by software and configured to generate an interrupt in case of an over temperature condition.

Chip Scale Atomic Clock (CSAC)

The VPX3-673 includes a high-stability CSAC which can be disciplined to a reference clock from either a GPS, an external device or from PTP over the network. The CSAC generates the disciplined clock source which is then distributed as radial clocks to the system.

Inertial Measurement Unit (IMU)

The VPX3-673 includes a 10 degree of freedom IMU on-board, which provides 3-axis accelerometer, gyro and magnetometer, along with a barometric pressure sensor. The IMU is connected to the processor and can be used to track position and movement information.

GPS

The VPX3-673 supports an on-board GPS Receiver (SAASM GB-GRAM Type II, upgradeable to M-Code). The GPS position is provided to the CPU and a 1 PPS clock output is used to discipline the CSAC, which in turn sources the clock synchronization and distribution circuitry.

Security Features

The VPX3-673 has been designed to support a powerful and flexible set of Trusted COTS (TCOTS) features. Security features include hardware and software capabilities designed to protect critical resources from unauthorized access or modification.

Arm v8 cryptography extensions

The VPX3-673 Arm processor provides support for AES encryption and decryption, as well as SHA-1, 224, 256 and finite field arithmetic for additional cryptography algorithms (E.g. elliptic curve).

UEFI Secure Boot

The VPX3-673 includes support for UEFI Secure Boot. Secure Boot extends the secure boot process to validate the OS boot loader, and then extends security into the operating system.

NXP Secure Boot/SEC 5

The LS0143A implements NXP's QorIQ platform's Trust Architecture 2.1, supporting trusted boot and maintenance of trusted architecture during run time. The Trust Architecture 2.1 is distinguished from previous versions of the QorIQ platform's trust architecture through the complementary inclusion of the Arm TrustZone, as appropriate to the needs of secure network and access infrastructure. The details of the Trust Architecture be found in the LS1043A reference manual.

Software Support

The VPX3-673 is supported by Uboot, firmware, and NXP Linux SDK Operating Systems with RTOS board support packages (BSP) from Curtiss-Wright. Systems developers will be able to kick-start application development using a common set of features and software interfaces across many products from Curtiss-Wright. For A-PNT applications, Curtiss-Wright's Common A-PNT Software Load (CASL) is available in a U.S. DoD variant.

Specifications

The VPX3-673 is available in Level 200 (-40 to +85°C) conduction-cooled ruggedization level with a 1" pitch. Full details of Curtiss-Wright's standard Ruggedization Guidelines can be found on the Curtiss-Wright website.

TABLE 6 Dimensions and weight

Option	DIMENSIONS	WEIGHT (GRAMS)
Conduction-cooled	ANSI/VITA 65 / 48. 1" Pitch	450

Notes:

1. Conduction-cooled cards available in temperature Level 200.
2. Refer to Ruggedization Guidelines data sheet for more information.

Power Consumption

See Table 7 for power consumption for the VPX3-673 standard product variant basecards. Power consumption increases as operating temperature rises.

The VPX3-673 is designed to run off 5V and does not draw current from the other voltage rails for normal operation. Hence, power consumption in the table below is for 5V only.

TABLE 7 Variant Power Requirements

RUGGEDIZATION LEVEL	PART NUMBER	REFERENCE CONFIGURATION	WORST CASE TYPICAL POWER (W)
Level 200, conduction-cooled	VPX3-673-C4551101E	TBD	30 (estimated)

Notes:

1. Typical power is measured power while running stress test software that exercises CPU and board functions. The actual power consumption observed will vary by application.
2. For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption values.
3. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption values.

TABLE 8 Variant Power Requirements

VOLTAGE	PART NUMBER	MAX TYPICAL CURRENT AMPS	COMMENTS
+5V	Conduction-cooled Level 200	6.3A (TBC)	
+3.3V	Conduction-cooled Level 200	Not used	
+/- 12V	Conduction-cooled Level 200	Not used	
+ 3.3V_AUX	Conduction-cooled Level 200	< 200ma (TBC)	

Notes:

1. For thermal design considerations, Curtiss-Wright recommends adding 5% to the typical power consumption values. For power supply sizing, Curtiss-Wright recommends adding 20% to the typical power consumption values. This table provides card requirements and does not include mezzanine usage.
2. For worst case typical power, divide the power in watts by 5.

Ordering Information

To order the VPX3-673, please contact Curtiss-Wright Defense Solutions.