



# XMC-442

## XMC FPGA Accelerator

### Signal Processing Platform



#### Features

- ◆ XMC (VITA 42) FPGA signal processing accelerator
- ◆ One user-programmable Xilinx® Virtex®-5 FPGA (SX50T or SX95T)
- ◆ One bank of 275MHz DDR2 SDRAM (256MB total)
- ◆ Two banks of 275MHz QDR-II+ SRAM (18MB total)
- ◆ PCI Express® (4-lane) host interface
- ◆ Two configurable RocketIO™ (4-lane) ports
  - One to front panel or base card (Pn6)
  - One to base card, selectable Pn4 or Pn6
  - Up to 2.5GB/s bidirectional bandwidth each
- ◆ Up to 80-bits LVDS/LVTTL configurable as 40-pairs to the front panel
- ◆ 48-bits LVDS/LVTTL, configurable as 24-pairs LVDS to Pn4 connector
- ◆ Personality module permits custom front panel connector options
- ◆ Continuum FXtools FPGA design kit with:
  - Highly-optimized VHDL libraries
  - Reference designs
  - Scriptable SystemVerilog (IEEE 1800™) simulation testbench
- ◆ On-board PROM for FPGA configuration file storage
- ◆ SelectMAP interface for dynamic FPGA loading when used on CHAMP-FX2
- ◆ Support for ChipScope™ Pro interface

#### Supported Curtiss-Wright boards:

- CHAMP-AV6 Quad Freescale Power Architecture MPC8641
  - CHAMP-FX2 FPGA Accelerator
  - VPX6-185 Freescale MPC8641 SBC
  - VPX6-215 ExpressReach XMC/PMC carrier
  - VPX3-127 Freescale MPC8640 SBC
  - SVME-184 Freescale MPC8641 SBC
  - SVME/DMV-1901 Core Duo SBC
- ◆ Range of air- and conduction-cooled versions available

#### Overview

The XMC-442 is a reconfigurable computing platform designed to tackle demanding tasks such as image processing, radar, data compression, and signal intelligence. The logic resources and dedicated multiply/accumulate units within its Xilinx Virtex-5 SXT family FPGA allow highly parallelized processing designs which can dramatically accelerate the core algorithms common to many signal and image processing applications. Many algorithms such as FFTs, 1D and 2D convolutions and filters may be efficiently implemented in FPGAs, outperforming conventional microprocessor implementations with respect to size, power and cost.

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The XMC-442 is designed to augment the signal processing power of a host board. System implementations can range from a single SBC/XMC-442 combination to high-performance VPX systems with multiple CHAMP-AV6 and CHAMP-FX2 host cards, XMC-442's and other VPX-based processor and I/O cards. The Virtex-5 SX50T and SX95T FPGAs are specifically designed for numerical processing with a large number of multiplier units (Xilinx DSP48E slices) which are heavily used in DSP algorithms. To complement the processing power of the FPGAs, the XMC-442 has a variety of high-speed serial and discrete interfaces. Interfaces protocols including PCI Express® (PCIe), Serial RapidIO® (SRIO), Xilinx Aurora™ (RocketIO™) are all supported on the serial connections.

The development of FPGA IP can be a challenging engineering task. Curtiss-Wright offers the Continuum FXtools design kit to speed this effort and reduce the risk of missed development schedules. The FXtools kit provides a rich set of FPGA-based functions enabling rapid prototyping and deployment of FPGA-based systems. The toolkit contains a library of highly-optimized VHDL IP blocks including dual-port memory controllers, PCIe core wrapper, scalable switching interconnect, and advanced DMA engines. Based on the Xilinx ISE/EDK design flows these blocks can be combined with other off-the-shelf or custom IP blocks to implement custom signal, image, or I/O processing. FXtools also includes a set of design templates and example designs, as well as a SystemVerilog-based (IEEE 1800™) simulation testbench with a full set of bus functional models

and scripting capabilities. The XMC-442 provides a JTAG header to support the use of Xilinx ChipScope Pro and JTAG development tools. Refer to the Continuum FXtools datasheet for more details.

## Architecture

The XMC-442 architecture is suited to DSP applications that place a high premium on sustained I/O throughput, FPGA memory bandwidth and off-board fabric connectivity. The data flow capabilities of the XMC-442 ensure that applications can extract the most from the raw computing performance of the Virtex-5 FPGA. The XMC-442 architecture encompasses a number of key attributes that contribute to maximizing DSP performance:

- ♦ One Virtex-5 SXT platform FPGA
- ♦ A high-speed PCIe interface to host cards with VITA 42.3 XMC support
- ♦ High-speed Serial I/O to the XMC I/O connector (Pn6) with up to 5GB/s bidirectional bandwidth. Can support PCIe, SRIO and Aurora interface protocols
- ♦ High-speed Serial I/O to the front panel via an Infiniband connector with up to 2.5GB/s bidirectional bandwidth. Can support PCIe, SRIO and Aurora interface protocols.
- ♦ 6.6GB/s peak memory bandwidth to the FPGA using one DDR2 SDRAM bank and two QDR-II+ SRAM banks
- ♦ Out-of-band control bus for FPGA application command and control when mounted on a CHAMP-FX2
- ♦ On-command FPGA reconfiguration

Table 1: XMC-442 Virtex-5 SXT capabilities

	CLB Resources				Memory Resources			Clock Resources		Embedded Hard IP Resources	
	CLB Array Size (Row x Column)	Slices	Logic Cells	CLB Flip-Flops	Max Dist. RAM (kbits)	Block RAM / FIFO w/ECC (36-kbits each)	Total BRAM (kbits)	Digital Clock Manager (DCM)	Phase Locked Loop (PLL) / PMCD	DSP48TM slices	PCIe Endpoint Blocks
SX50T	120x34	8,160	52,224	32,640	780	132	4,752	12	6	480	1
SX95T	160x46	14,720	94,208	58,880	1,520	244	8,784	12	6	640	1



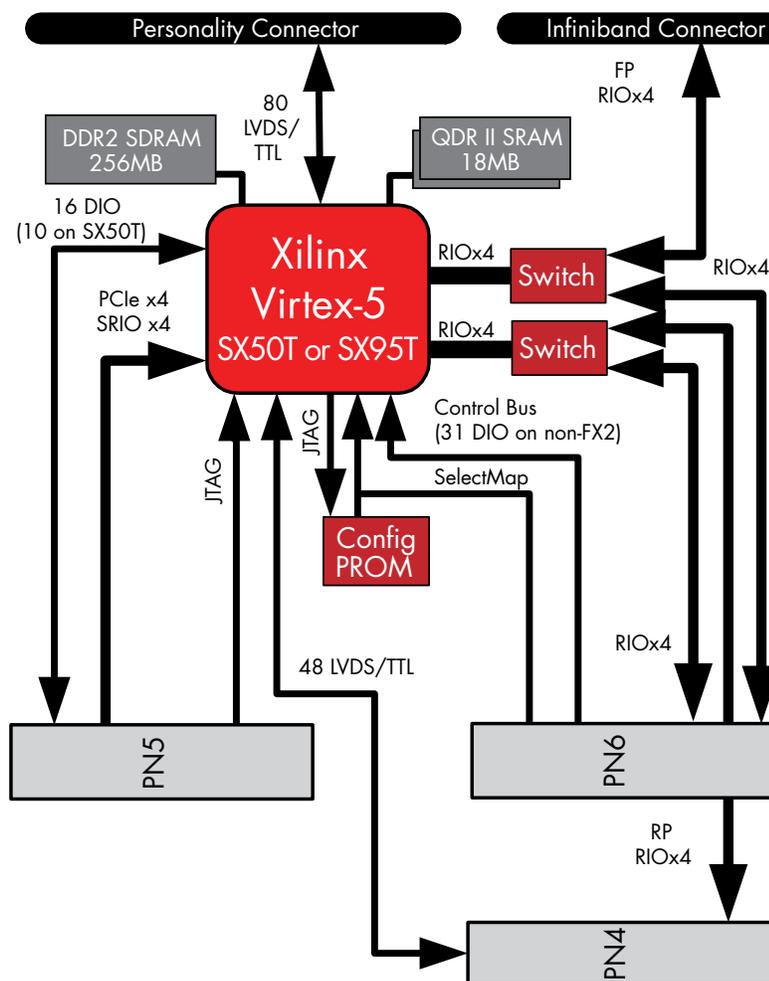
## Virtex-5 SXT Details

The XMC-442 can be fitted with the highest gate-count versions of the Virtex-5 SXT family. Each device contains a high density array of logic cells, DSP48E slices, and multiple on-chip memory banks that enable high-speed vector processing. These FPGAs allow multi-gigabit/s connectivity for high-bandwidth, low-latency communication. The table below highlights the Virtex-5 SXT capabilities found on the XMC-442.

The Virtex-5 SXT offers a number of features that are either enhancements over earlier generation Virtex components or are entirely new to the Virtex-5. The 65nm ExpressFabric™ logic gate technology of the Virtex-5 is the first to use a 6-input LUT which provides higher speed, lower power,

and lower resource usage than earlier FPGA generations. The Distributed RAM is a 256-bit memory per CLB with 64-bits per LUT, while the Block RAM has been increased to 36Kbit dual-port blocks with independent clocking on each port. The BRAM memories can be easily configured as single-port, dual-port, or FIFO memory structures and are instrumental in achieving high performance in DSP applications. The DSP48E slices have been enhanced with a 25 x 18 multiplier and a 48-bit adder to enable single-precision floating point math and wide filters with fewer slices. These features are combined with various power-saving features to make the Virtex-5 SXT an ideal choice for high-performance embedded computing.

Figure 1: XMC-442 User FPGA External I/O and Memory Interfaces





## User FPGA Architecture

The user FPGA has a variety of external I/O and memory interfaces as shown in Figure 1. Some or all of the following interfaces may be implemented in a user FPGA design:

- ◆ Up to two independent QDR-II+ SRAM interfaces
- ◆ One DDR2 SDRAM interface
- ◆ Up to three high-speed 4-lane serial interfaces supporting PCIe, SRIO, Aurora protocols
- ◆ Discrete I/O (LVDS or LVTTL)
- ◆ Control bus interface

## DDR2 SDRAM

The FPGA node offers a 256MB, 32-bit wide bank of 275MHz DDR2 SDRAM. The peak bidirectional data transfer rate to this memory is 2.2GB/s. Typical uses for the SDRAM include temporary data storage, historical data storage, or as a scroll buffer. The SDRAM IP Block included in the Continuum FXtools toolkit supports using the SDRAM as an addressable RAM, a generic FIFO interface or a circular data buffer.

## QDR-II+ SRAM

The FPGA node offers two 9MB, 18-bit banks of 275MHz QDR-II+ SRAM for a total of 18MB. The instantaneous peak bidirectional data transfer rate for these memories is 4.4GB/s. The SRAM is suitable for temporary data storage associated with DSP algorithms like FFTs or filters. The SRAM IP Block included in the Continuum FXtools toolkit supports using the SRAM as an addressable RAM or a generic FIFO interface.

## XMC (VITA 42)

The VITA 42 standard and subsidiary specifications define the XMC mezzanine module format which adds high-speed data interfaces and I/O capability to the PMC standard. The XMC-442 employs the Pn5 (host interface) and Pn6 (XMC I/O) connectors defined in the standard to provide significantly higher performance than possible with the PMC standard.

The host interface of the XMC-442 supports a 4-lane PCIe (VITA 42.3) interface, providing up to 2GB/s peak bidirectional bandwidth. Using the optional SRIO IP, the

XMC-442 can be configured to provide a 4-lane SRIO host interface (VITA 42.2). This enables the FPGA to be an end-point in a SRIO fabric system when the host card extends the SRIO fabric to its XMC connectors. The CHAMP-FX2 and VPX6-185 SBC provide this capability.

Table 2: The XMC-442 is compatible with the following Curtiss-Wright host boards

Product	Form-Factor	Host Interface	I/O interface
CHAMP-AV6 Quad Freescale MPC8641	6U VPX	Single site, PCIe x4	Pn4, Pn6
CHAMP-FX2 FPGA Accelerator	6U VPX	Single site, PCIe x4	Pn4, Pn6
VPX6-185 Freescale MPC8641 SBC	6U VPX	Dual sites, PCIe x4	Pn4, Pn6
VPX6-215 Express Reach XMC/PMC Carrier	6U VPX	Dual sites, PCIe x4	Pn4, Pn6
VPX3-127 Freescale MPC8640 SBC	3U VPX	Single site, PCIe x4	Pn4
SVME/DMV-184 Freescale MPC8641 SBC	6U VME	Single site, PCIe x4	Pn4
SVME/DMV-1901 Core Duo SBC	6U VME	Single site, PCIe x4	Pn4

The XMC-442 is a single-width XMC module. Air-cooled modules are designed in accordance with the IEEE 1386 and 1386.1 specifications. Conduction-cooled modules are designed in accordance with ANSI/VITA 20-2005, Conduction-cooled PCI Mezzanine Standard. The cooling surfaces provided are the Primary Thermal Interface Region and the side 1 Secondary Thermal Interface Regions.

## Serial RocketIO Connectivity

The XMC-442 provides a pair of high-speed serial I/O ports based on Xilinx' RocketIO GTP technology. These 4-lane ports operate at up to 3.125GB/s providing 2.5GB/s bidirectional bandwidth each. The XMC-442 features user selectable routing of the RocketIO ports to support connections to the front panel, the XMC Pn6 high-speed connector or the Pn4 connector. The routing options are as follows:

- ◆ Port1: Pn6 or Pn4 connector.
- ◆ Port2: Pn6 or front panel Infiniband style connector



The RocketIO ports may be configured to provide a variety of protocols including Xilinx Aurora, PCIe or SRIO. Note that the Pn4 connector is not designed for high data rates and is recommended for maximum signaling rates of 1GB/s or less.

## FPGA Configuration & the SelectMAP Interface

The XMC-442 contains a rewritable serial PROM which can be loaded with a custom bit-stream for FPGA configuration at boot time. This PROM may be loaded via JTAG or through a basecard user API. When the XMC-442 is mounted on a CHAMP-FX2, however, the SelectMAP interface allows the FPGA to be configured directly from the Freescale processor on the CHAMP-FX2 basecard. This feature allows application developers to dynamically reconfigure the FPGA on-command during system operation.

## Command Bus

The XMC-442 supports a command bus interface on the Pn6 connector. This is an out-of-band communications bus that may be used to give command and control instructions to the user FPGA without interfering with data movements in or out of the primary high-speed serial interfaces. The command bus is supported on the CHAMP-FX2.

## LVTTTL/LVDS Discrete Digital I/O

The XMC-442 supports discrete I/O signals that are available on the front panel and Pn4 connector. These signals may be configured by the FPGA load to provide 2.5V or 3.3V LVTTTL single-ended or 2.5V LVDS differential pair signaling. The front panel provides 80 LVTTTL or 40 LVDS pairs, while the Pn4 provides 48 LVTTTL or 24 LVDS pairs.

## Thermal Sensor

The XMC-442 utilizes the internal Virtex-5 thermal sensor as well as an external sensor to give applications the means to monitor the temperature of the mezzanine board. Accessed through APIs on the base card, these sensors can be read by application software and are accurate to  $\pm 2.5^{\circ}\text{C}$  from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . A temperature alert signal is connected to the FPGA.

## Current Sensor

The XMC-442 provides a current sensor to measure the total current drawn by the mezzanine board. Utilizing the Virtex-5 System Monitor and accessible through APIs on the base card this sensor gives the developers the means to tune their application to meet often demanding power limits found on deployed systems.

## XMC-442 Front Panel

Air-cooled XMC-442 modules provide the following optional front panel provisions:

- ◆ Infiniband-style receptacle connector for RocketIO, FCI part number 10009629102010 or equivalent incorporating EMI gasket and threaded standoffs
- ◆ A Samtec QSH-series connector breaking 80 discrete I/O signals to a “personality module” that can be customized for different user requirements.

## Continuum FXtools

Continuum FXtools is the developer’s kit for the XMC-442 and includes the following functionality:

- ◆ XMC-442 Hardware, Software, and FPGA User’s Manuals
- ◆ High-performance IP block library
- ◆ Example reference designs
- ◆ SystemVerilog (IEEE 1800) simulation testbench
- ◆ Support for Xilinx ISE and ChipScope Pro tools
- ◆ Software driver library

Refer to the Continuum FXtools datasheets for more details.

## Options

Contact the factory for configurations options.



## Specifications

The XMC-442 is available in a full range of environmental grades starting from commercial air-cooled to extended temperature, rugged, conduction-cooled versions. This allows the customer to select the board to match the environmental requirements of the platform. The tables below show the power, dimensions and weight of the board.

Table 3: Maximum and Typical Power

FPGA complement	Maximum power			Typical power		
	12V	5V	3.3VAux	12V	5V	3.3VAux
SX55T	0W	13W	0.1W	0W	10W	0.1W
SXT95	0W	17W	0.1W	0W	14W	0.1W

Table 4: Weight

Option	Dimension	Weight
Air-cooled	Per IEEE 1386	119g
Conduction-cooled	Per ANSI/VITA 20-2005 Incorporates Primary Thermal Interface Region and the side 1 Secondary Thermal Interface regions.	144g

## Warranty

This product has a one year warranty.

## Contact Information

To find your appropriate sales representative, please visit:

Website: [www.cwembedded.com/sales](http://www.cwembedded.com/sales)

Email: [sales@cwembedded.com](mailto:sales@cwembedded.com)

For technical support, please visit:

Website: [www.cwembedded.com/support1](http://www.cwembedded.com/support1)

Email: [support1@cwembedded.com](mailto:support1@cwembedded.com)

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