



XCLK1

Ultra Low Jitter 2 GHz Multi-Channel Clock Generator

Applications

The XCLK1 is an ideal source for analog to digital converter sample clock for DSP applications including:

- ◆ Signal Intelligence (SIGINT)
- ◆ Spectral Analysis
- ◆ Radar

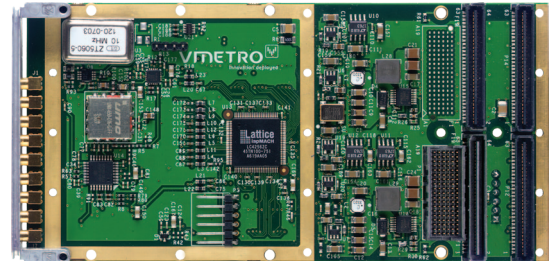
Features

- ◆ 6 phase matched RF outputs (6 single-ended or 3 differential)
- ◆ Selectable internal or external 10 MHz reference (with frequency multipliers for RF output)
- ◆ External RF clock source
- ◆ XMC/PMC format (power only)
- ◆ Air-cooled and rugged build options

Benefits

- ◆ Provides a low cost, small form factor solution for low jitter clock sources
- ◆ Enables ease of synchronizing multiple acquisition cards
- ◆ Industry standard form factor
- ◆ For use in deployed or commercial environments

Overview



High-speed analog I/O solutions require good quality sample clock sources – often with multiple phase matched feeds to support an array of I/O converters. Such products are often expensive, bulky and not suited to embedded environment. The XCLK1 is different because it was designed with embedded computing in mind by providing a clock source, with up to six phase matched outputs, packaged in a convenient PMC or XMC board form factor.

The XCLK1 offers a number of clock source options including an internal temperature compensated crystal oscillator or off-board RF or off-board 10 MHz references. The 10 MHz reference sources are used to drive low phase noise VCO/PLL frequency multiplication circuitry (each frequency output is a build variant). Local frequency multiplication based on the 10 MHz temperature compensated crystal oscillator (TCXO) can generate output signals in the range of 500 MHz to over 2 GHz with a jitter of less than 0.5ps. Single-ended and differential clock outputs are supported.

When providing a clock source to multiple acquisition cards, users often need to synchronize the trigger or start of acquisition for all cards so that multiple samples across different ADC or DACs are coherent. This is important for applications such as beamforming. The XCLK1 helps solve this problem by being able to momentarily interrupt all sample clock outputs using its trigger/reset input. This gives time for all acquisition cards to be reset and to start to capture data synchronously.

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Figure 1: The XCLK1 can synchronize multiple analog input PMC/XMCs such as the AD3000

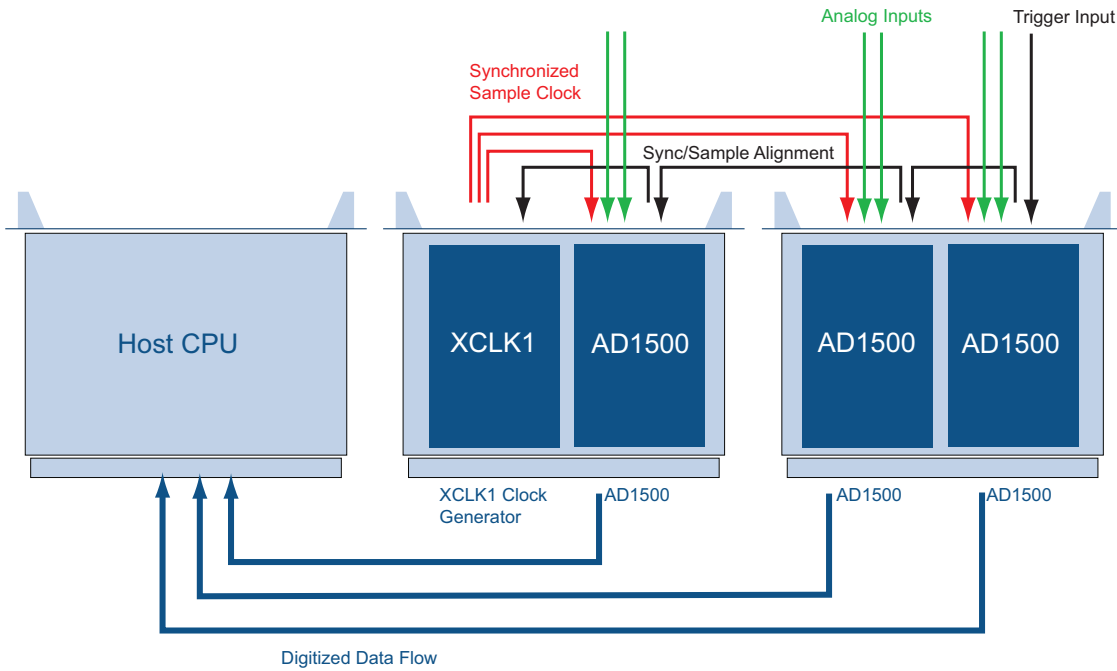
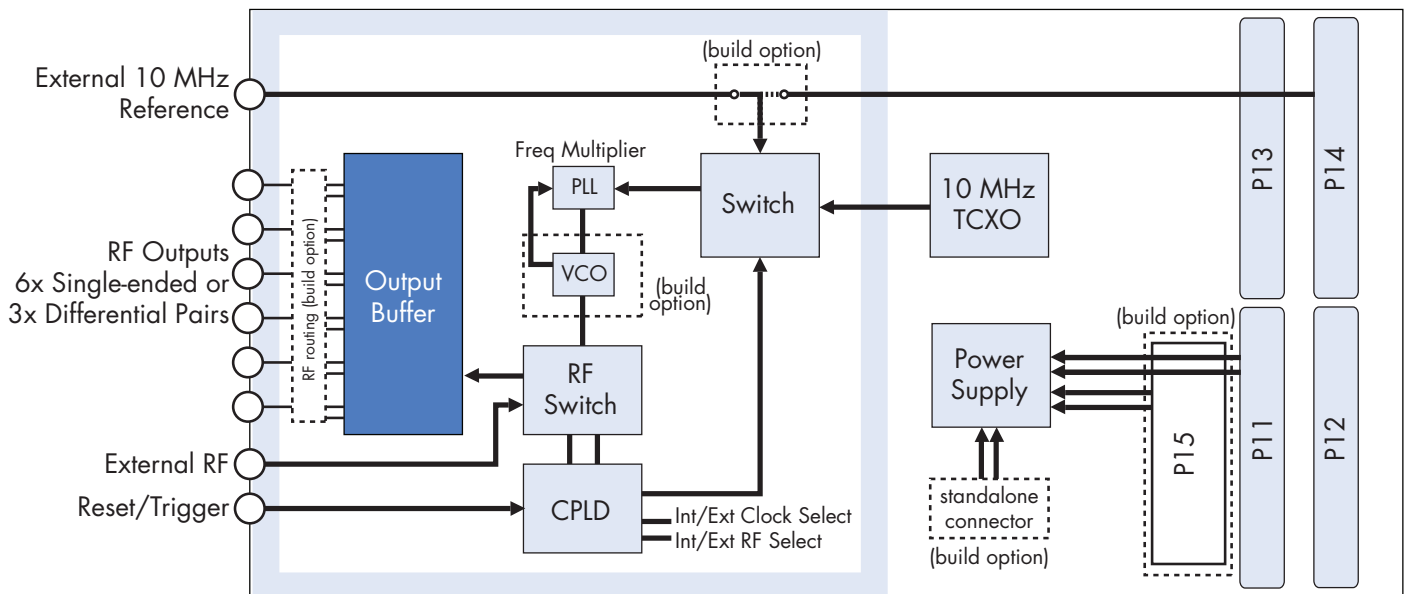


Figure 2: XCLK1 Block Diagram



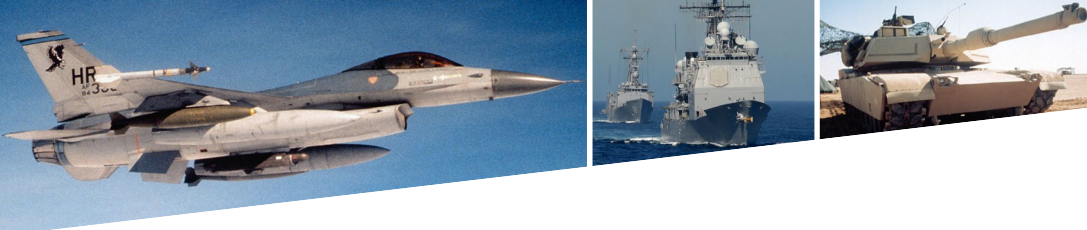


Table 1: Specifications

RF Clock Outputs	
Number of Channels	6 Single-ended or 3 Differential (build option)
Connectors	Front Panel MMCX
Output Level	50 Ohm, AC coupled, LVPECL 500-700mV (typ)
Internal Reference	
Frequency	10 MHz
Typical Phase Noise	Offset dBc/Hz
	10 Hz -105
	100 Hz -135
	1 kHz -155
	10 kHz -163
100 kHz -165	
External 10MHz Reference (front panel)	
Input Level	50 Ohm AC coupled -5 to +5 dBm recommended
Connector	Front panel MMCX
External 10MHz Reference (PMC User I/O) - Build Option	
Input Level	100 Ohm DC coupled ±200 mV recommended
Connector	PMC P14 User I/O
External RF Clock Input	
Output Level	50 Ohm AC coupled -5 to +5 dBm recommended
Frequency Range	0-2 GHz
Connector	Front panel MMCX
Reset/Trigger	
Input Level	LVPECL
Connector	Front panel MMCX
Power	
Supply	3V3 (2.5 W) & GND PMC P11, XMC P15 or stand alone (build options)
Misc	
Weight	Air-cooled: 90 g Conduction-cooled: 70 g
MTBF	4,545,000 hours (Note 1)
Environmental	
Air-cooled	AC L0, AC L100 (see Curtiss-Wright ruggedization table)
Conduction-cooled	CC L100 (see Curtiss-Wright ruggedization table) Note: host heatframe will require modification for front panel I/O

Note

1. Calculated using 217Plus, inherent model. GB environment @ 30 deg C

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwembedded.com/sales

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Technical Support

For technical support:

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