Data Sheet

VPX6-6902

Serial RapidIO® and Ethernet Combined Switch

Features

- 6U OpenVPX™ centralized switch for Serial RapidIO® (SRIO) Data Plane and Ethernet Control Plane
  - OpenVPX/VITA-65 compliant design supports 24F, 16U20F and 20U19F switch profiles
- Available with SRIO switch fabric alone, or combined SRIO and Ethernet switches in a single-slot
- Enables easy implementation of scalable high-performance centralized DSP clusters for small, medium and large systems
- Supports star and dual-star topologies
- SRIO Data Plane Features
  - 19, 20, or 24 SRIO 4-lane (x4) ports to the VPX backplane + 4 ports to the front (AC models)
  - Each SRIO port is capable of operating at Gen1 speeds of 1.25, 2.5 and 3.125 Gbaud or Gen2 speed of 5.0 Gbaud
- Ethernet Control Plane Features
  - Full line-speed non-blocking 76 Gbps core switching architecture
  - 16 or 20 ports 1000Base-X (SerDes) plus 2 ports 1000Base-T to the backplane
  - 2 ports 10GbE XAUI plus 1 port 1000Base-T to the front panel (AC models)
  - High-performance Layer 2 Switching Functionality
    - Up to 4K VLANs
    - Jumbo frames up to 13KB
    - Spanning Trees including STP, RSTP, MSTP
    - Multicast support with IGMP snooping, MLD discovery
    - Link Aggregation and Port Mirroring, Automatic Flow Control
  - Onboard management processor for Ethernet fabric management
    - Independent out-of-band serial RS232 management port
    - In-band management (Telnet) through any Ethernet port
    - Dedicated 10/100Base-TX Debug port
- Declassification capability to return card to factory configuration
- Extensive Built-in Test (BIT) features
  - PBIT for power-up full system test
  - CBIT for continuous non-intrusive Ethernet system monitoring
  - IBIT for user-initiated on-demand Ethernet tests
- IPMI support
  - Intelligent Platform Management Interface (IPMI) monitors and reports board status, power & temperature
  - Supports remote reset
- Field upgradeable software
- Air-cooled and conduction-cooled versions available

VPX™ OpenVPX™

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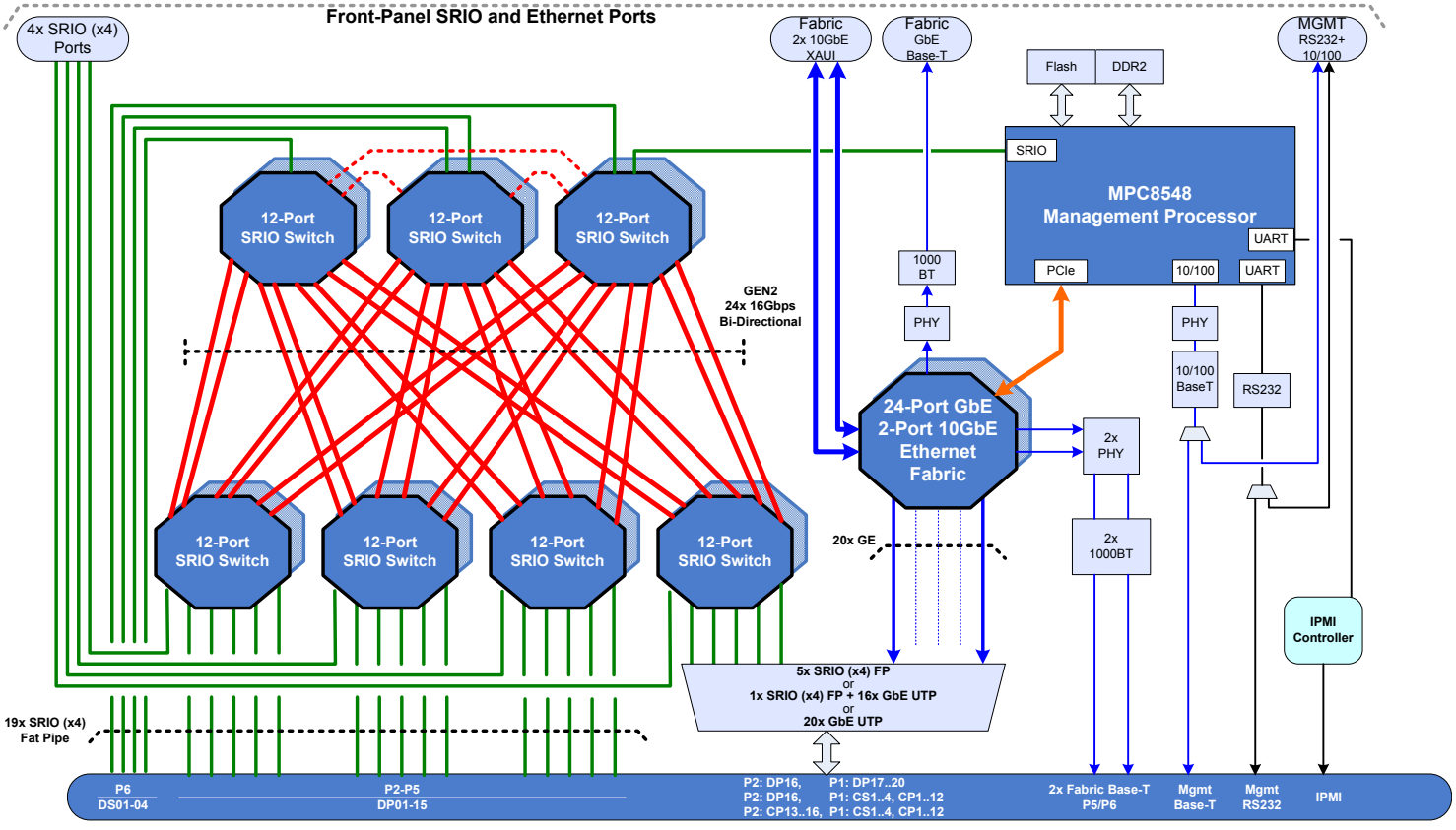
Overview

The VPX6-6902 is a combined management, control and data plane switch for small, mid-size and large 6U VPX systems. Supporting a centralized switch architecture in both star and dual-star topologies, the VPX6-6902 is available with SRIO switching alone, or with both SRIO dataplane and Ethernet management/control plane switching all in a single VPX slot.

The VPX6-6902 allows systems integrators to architect small to large high-performance systems following the guidelines provided in the VITA-65 (OpenVPX™) systems specification. It can be used in multiple backplane profiles, with up to 24 4-lane Fat Pipes (FP) for SRIO and up to 20 Ultra-Thin Pipes (UTP) for SerDes Gigabit Ethernet on the backplane. Additional SRIO and Ethernet ports are available on the front panel for air-cooled modules.

The VPX6-6902 complements a wide range of Curtiss-Wright Controls Embedded Computing VPX modules, including DSP, FPGA, and CPU single board computers, allowing systems integrators to implement extremely high-performance data, control and management plane systems.

Figure 1: VPX6-6902 SRIO and Ethernet Switch



Backplane P0 ~ P6

Serial RapidIO Data Plane

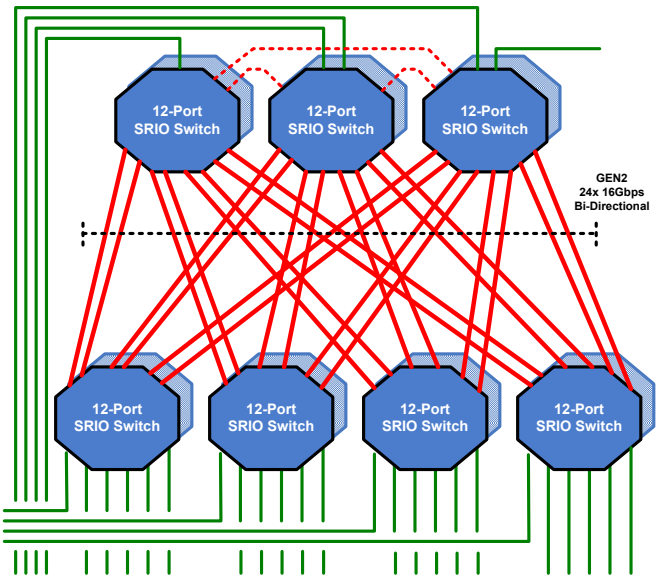
The VPX6-6902 uses the latest generation of high-performance SRIO packet processing switch fabrics. Utilizing an array of seven 48-lane Gen2 devices, the VPX6-6902 supports up to 28 SRIO connections. Each connection supports 4-lane operation (x4), and is backwards compatible with x2 and x1 SRIO interconnects.

Each SRIO connection supports SRIO Gen1 and Gen2 traffic. Gen1 connections operate at 1.25, 2.5, or 3.125 Gbps rates (per lane) and Gen2 connections can operate at 5.0 Gbps rates (per lane). When operating in x4 lane mode at 5.0 Gbps, each SRIO x4 port supports a sustained payload throughput of 16 Gbps in each direction. With 28 device connections, the VPX6-6902 supports an impressive aggregate data throughput of over 896 Gigabits per second.

Internal switch-to-switch links operate at the full 5.0 Gbps x4 rates, and with multiple links available for each device-to-device connection, a total of 768 Gbps of internal fabric switching is supported.

Each switch device offers cut-through and store-and-forward operational modes, with packet latency as low as 100ns. Advanced SRIO features such as multicast, mirror/trace and multiple levels of packet priorities are also supported.

Figure 2: Serial RapidIO Switching Fabric



Serial RapidIO Software Support

While the VPX6-6902 contains an Ethernet management processor, it is possible to fully exploit the board's full switching capabilities without running any software on the VPX6-6902 itself. RapidIO fabrics can be initialized and configured by any attached processing end-point. Data movement can be implemented using low-level hardware-aware BSP calls or a portable middleware such as the IPC inter-processor communications library. System level analysis and debug is facilitated through the use of the fabric development tool Continuum Insights.

VxWorks® BSP Support for Serial RapidIO

The Board Support Packages (BSPs) for Curtiss-Wright SBC, DSP and FPGA boards provide functions that initialize, configure, operate, test and troubleshoot the hardware modules in the system. The BSP also contains example code which enumerates the Serial RapidIO fabric, assigning a unique device id to each processing element. Additionally, a host processor can configure switches in the fabric by using RapidIO maintenance packets.

BSP Data Movement

Board support packages include an application programming interface (API) which performs all of the basic functionality needed to set-up and move data over the RapidIO fabric. High-performance inter-board transfers are supported using Remote Direct Memory Access (RDMA) and kernel bypass mechanisms to deliver highly efficient wire-speed data movement for distributed processing systems.

API functions are provided for:

- Fabric enumeration/device discovery
- Configuring mapping windows in support of global addressing (RapidIO IO Logical Layer)
- Message passing (RapidIO message passing logical layer)
- Doorbells (RapidIO's mechanism for asynchronous device notification)
- Error handling

The software developer may build signal processing applications entirely using the RapidIO API that is included with the board support package. Simple data flows are easily supported in this straightforward manner. Complex applications with more sophisticated data flows may be more portable and much simpler to develop and maintain

using a higher-level message passing middleware that is architected to abstract the system and maintain overall system coherency.

Continuum IPC Library

In order to abstract away from the hardware architectural details of interconnected SRIO systems and to make use of the richer feature set offered by SRIO, Curtiss-Wright offers our Continuum IPC Inter-Processor Communications Library. This software provides all the capabilities needed to control applications running on multiple processors having data movement requirements. Continuum IPC software hides the hardware architectural details from the application designer, allowing for example, message passing functions to send messages using the same application interface and parameters, whether the destination task resides on the same processor, same board, or any other board interconnected across the SRIO fabric. The hardware abstraction provided by Continuum IPC ensures that applications written for current generation processors and fabrics will be easily portable to the next generation. The library determines the location and end-point addressing for source and destination as applications open endpoints for input (receiving messages) or output (sending messages). With routing information stored within each processor, the software does not impose a single point of failure as would result from a centralized table of buffer or destination mapping information.

Users can perform message passing across SRIO fabrics using POSIX-style open, close, read and write functions, and can be qualified as priority-based, queue-driven, flow-controlled and reliable. Bulk data transfers become simple to use, as one application creates a receive buffer, and announces it to the network by providing the buffer name, address, and size, and other processors open the buffer using the same name, for output operations. Write operations cause high-speed DMA transfers from the source processor's buffer to the destination buffer across the SRIO fabric. Bulk data transfer functions are optimized for high volume, low-latency data such as that which occurs in time-critical data flow architectures.

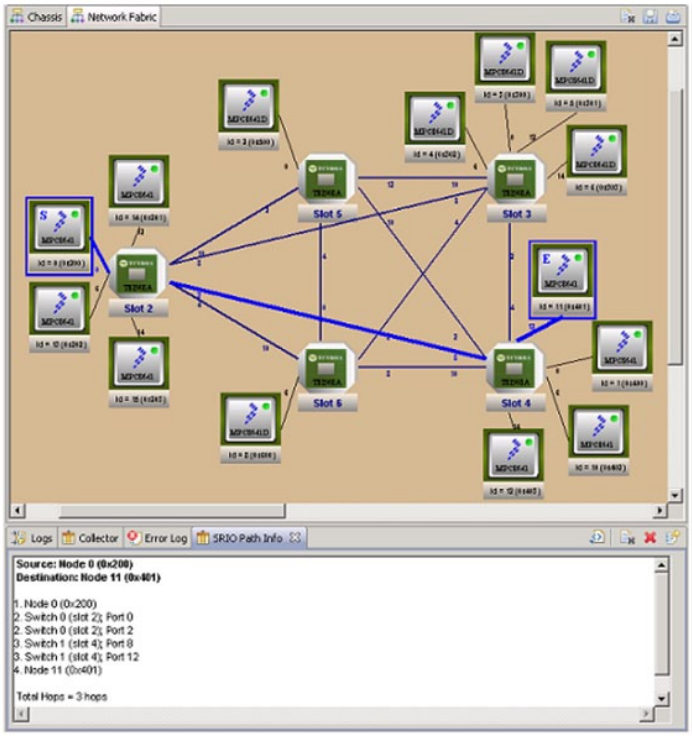
Continuum Insights

Curtiss-Wright also offers Continuum Insights, a suite of GUI-based software tools designed to ease and optimize the development of application software for multi-processor embedded systems. With support for systems ranging in size from tens to hundreds of interconnected processors and cores, developers gain access to unprecedented levels of information in regards to operational status and inter-processor interactions in an easy to use and navigate GUI format.

Continuum Insights is based on the Eclipse Development and Application Framework, and provides developers of complex multi-processor-based computer systems with the information they need to accurately tune their system and speed their time to market. This advanced suite of development tools includes an Event Analysis Tool, System Monitoring Tool, System Management Tool, Network Fabric Analysis Tool, and a Multi-Node Debugger.

Continuum Insights is fully SRIO fabric aware, and the Fabric Analysis Tool provides features such as interconnect and topology analysis, route display and assignment, network path trace, and SRIO switch and node status and statistics. Continuum Insights can also monitor SRIO path performance, ensuring data paths are configured optimally and are not overloaded or used beyond capacity. The quantity and nature of the SRIO traffic can be analyzed including information on packet priority classes, uni-cast and multicast packets and control symbols. Congestion statistics are available that measure the occurrence of switch input/output queues reaching a specified depth threshold. A variety of error statistics are accessible including rate of CRC errors and number of dropped packets. Between the performance and error statistics, a user can determine if there are any underlying problems in the SRIO system and whether those problems are of a data congestion, or signal integrity nature. The user may examine the performance and error statistics ad-hoc, or may setup the software to periodically poll and store the information to a file for later analysis.

Figure 3: Example Screenshot from Continuum Insights, Displaying an SRIO Network Topology



With these tools, configuring and developing an SRIO connected topology using the VPX6-6902 is greatly simplified. Understanding precisely the intricacies of the complex multi-computer reduces development time and ultimately speeds time to market.

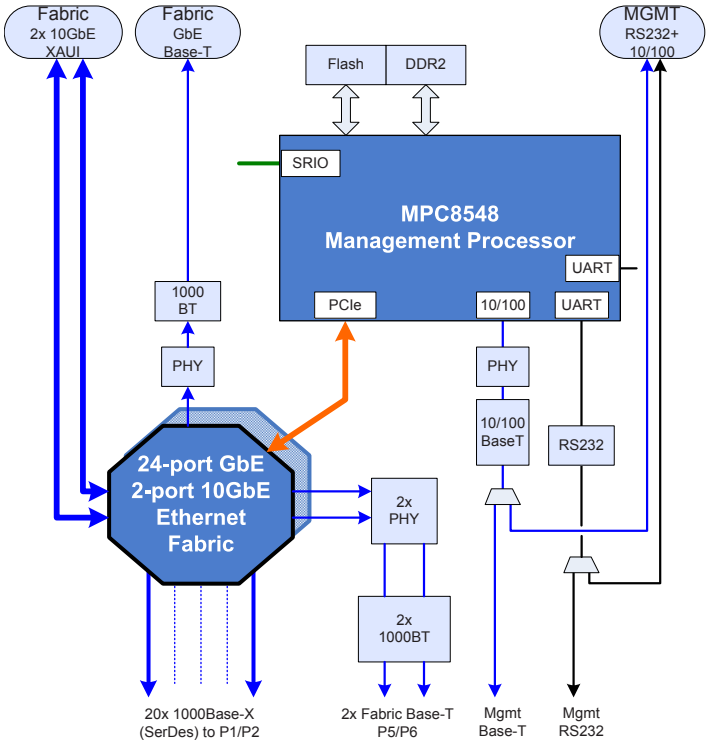
Ethernet Control Plane

The VPX6-6902 features an Ethernet control plane switch. Based on the industry leading Broadcom® StrataXGS® IV multi-layer switching fabric, the VPX6-6902 is capable of supporting line-rate non-blocked Layer 2 switching on all ports, supported by a core switching capacity of 76 Gbps. The key features at the core of the switching fabric that facilitate low latency wire-speed performance include 2 MB of high-speed fully integrated on-chip packet buffer memory, advanced Content-Aware packet processing, and advanced packet flow control capabilities.

Depending on the model, either 16 or 20 ports of SerDes 1000Base-X Ethernet is provided to the backplane for payload modules. The use of a SerDes connection uses half the number of signal lines as traditional 1000Base-T interfaces, and increases reliability due to the absence of bulky signal transformers. Two additional 10/100/1000Base-T ports are provided on the backplane, and can be used for additional payload modules, or for external Ethernet connections. For air-cooled boards, another 10/100/1000Base-T and two 10GbE XAUI (10GBase-CX4) control plane connections are provided on the front panel. The two 10GbE ports can be used to directly connnect high-speed sensors or data storage devices, or they can be used to create high-speed 10GbE backbones between multiple switches.

The VPX6-6902 supports a managed Layer 2 switching feature set that includes support for VLANs and multicast. Switch management can be performed in-band using any Ethernet port (via Telnet), or out-of-band using the module's serial RS-232 port.

Figure 4: Ethernet Switching Fabric





VPX Backplane Port Configurations

The VPX6-6902 is designed to be VITA-46/VITA-65/ OpenVPX compliant and is available to support several different OpenVPX module profiles and slot pinouts.

Table 1 (below) summarizes the port configurations offered, and indicate the port mappings to the VPX backplane P1-P6 connectors and module front panel (for air-cooled versions).

IPMI

The VPX6-6902 includes an Intelligent Platform Management Interface (IPMI), enabling system monitoring and management. On-board supply voltages and current, along with temperature measurements, can be queried by an IPMI system controller.

Additionally, the IPMI system controller can perform a hardware reset to the VPX6-6902 module.

Additional Features

Built-in Test (BIT)

The VPX6-6902 supports Powerup BIT (PBIT), Continuous BIT (CBIT), and Initiated BIT (IBIT) designed to detect system faults. PBIT tests both the Ethernet and SRIO systems. CBIT and IBIT operate on the Ethernet subsystem. BIT results are available through the IPMI Management interface, or through the RS-232 management port.

Declassification

All Curtiss-Wright routing products provide a Declassification utility that erases all non-essential content in the board's non-volatile flash memory. This process deletes all switching tables, filters and user configurations, purges the switches of Ethernet and SRIO packets, and restores the board to its factory default configuration. This feature provides an extra layer of security, often required when removing a module from service, and can also be used to recover a default configuration in the event of mis-configuration or corruption.

Table 1: VPX6-6902 Port Configurations

Part Number	OpenVPX Profile Supported	Cooling & Rugged Level	SRIO Switch				Ethernet Switch					10/100Base-TX Debug/Upgrade Port	
			Total # of Ports	Rear		Front	1000Base-X (SerDes) Rear		1000 Base-T	1000 Base-T	10 GbE XAUI	Front	Rear P3
				P2-P6	P1		P1	P2	Rear P5/P6	Front	Front		
VPX6-6902-A04123 VPX6-6902-A14123	MOD6-SWH-20U19F	AC L0 AC L100	23	19	0	4	16	4	2	1	2	1	1
VPX6-6902-C24119		CC L200	19			0				0	0	0	1
VPX6-6902-A04124 VPX6-6902-A14124	MOD6-SWH-16U20F	AC L0 AC L100	24	20	0	4	16	0	2	1	2	1	1
VPX6-6902-C24120		CC L200	20			0				0	0	0	1
VPX6-6902-A04028 VPX6-6902-A14028	MOD6-SWH-24F	AC L0 AC L100	28	20	4	4	No Ethernet switch						
VPX6-6902-C24024		CC L200	24			0							



Table 2: Hardware Specifications

Feature	Description
Switching Fabric	Broadcom StrataXGS IV 563xx series
Management/Control Processor	Freescale Power Architecture MPC8548 ◆ 512 MB DDR2 RAM ◆ 256+128 MB Flash
Ethernet Fabric Ports	Backplane Ports: ◆ 16 or 20 ports 1000Base-X (SerDes) ◆ 2 ports 1000Base-T (supporting 10Base-T, 100Base-TX, and 1000Base-T) Front Panel Ports (air-cooled only) ◆ 1 port 1000Base-T (supporting 10Base-T, 100Base-TX, and 1000Base-T) ◆ 2 ports 10GBase-CX4 (XAUI)
Ethernet Port Specifications	◆ 10Base-T interfaces per IEEE 802.3 ◆ 100Base-TX interfaces per IEEE 802.3u ◆ 1000Base-T interfaces per IEEE 802.3ab - auto MDI/MDIX crossover - max 100m segment length ◆ 1000Base-X interface per IEEE 802.3ap ◆ 10GBase-CX4 interface (XAUI) per IEEE 802.3ae
SRIO Fabric Ports	Backplane Ports ◆ 19, 20, or 24 ports Front Panel Ports (air-cooled only) ◆ 4 ports
SRIO Port Specifications	SRIO Port Width: ◆ Supports 4-lane, 2-lane and 1-lane operation (x4/x2/x1) Link Speed: ◆ Supports Gen-1 speeds of 1.25, 2.5, or 3.125 Gbps ◆ Supports Gen-2 speed of 5.0 Gbps
Debug Ports	10/100Base-TX Ethernet Port RS232 Serial Port
Power	SRIO Only: 55W (max) SRIO + Ethernet: 85W (max)
Form Factor	6U VPX
Environmental	◆ Convection (air-cooled): Available in levels 0 (AC L0) and 100 (AC L100) ruggedization - Required airflow is 15 CFM at sea level ◆ Conduction-cooled: Available at level 200 (CC L200) ruggedization *Unless otherwise noted environmental specifications are defined in Curtiss-Wright's Ruggedization Guidelines factsheet.*
Weight	Air-cooled: <TBD> g Conduction-cooled: <TBD> g

Table 3: Software/Functional Specifications

Feature	Specification
Layer-2 Switching Performance	76 Gbps aggregate switching performance
Capacity	◆ 2 MB Packet Buffer with dynamic buffer management ◆ Support for Jumbo Packets up to 13KB ◆ Up to 15K Layer-2 MAC Addresses ◆ Up to 4K VLANs ◆ Up to 1K Layer-2 Multicast groups
Layer 2 Switching Features	◆ GARP for LAN information ◆ VLAN routing and support ◆ VLAN broadcast, 802.1Q VLAN tagging & double-tagging ◆ Priority Based Switching (802.1p) ◆ GMRP for Multicast registration propagation ◆ IGMP MAC Snooping for forwarding of IPv4 Multicast traffic ◆ MLD MAC Snooping for forwarding of IPv6 Multicast traffic ◆ Link Aggregation (802.3ad, 802.1ax) for increased bandwidth and load sharing ◆ Port Mirroring ◆ Packet or byte-based rate limiting on a per-port basis ◆ IEEE 802.3x flow control and back-pressure support ◆ Loop-free topology via Spanning Tree Protocol (STP per 802.1D, RSTP per 802.1w, MSTP per 802.1s) ◆ MAC ACLs Filters ◆ LLDP (802.1ab -2005)
Other Features	◆ Ethernet switch configuration save and restore ◆ Management via CLI (serial port or in-band Telnet) with context-sensitive help ◆ Multi Level User Privileges and Login Authentication ◆ Declassification (secure memory/ configuration erase) ◆ Broadcast Storm Control
Built-in Test	◆ PBIT for powerup self-test ◆ IBIT for user initiated self-test ◆ CBIT for continuous self-test



Table 4: Ordering Information

The VPX6-6902 is ordered with the following part number guide.

VPX6-6902-uvwxyy	
VPX6	6U VITA 46 and 48 form factor
6902	Model number
u	Cooling Method A = Air cooled C = Conduction cooled
v	Ruggedization Level 0 = L0 (0 to 50°C) 1 = L100 (-40 to 71°C) 2 = L200 (-40 to 85°C)
w	Mechanical Format 3 = 0.85" pitch, 2-level maintenance support 4 = 1.0" pitch, no 2-level maintenance support 5 = 1.0" pitch, 2-level maintenance support
x	Ethernet Functionality 0 = no Ethernet functionality 1 = Layer 2 Ethernet functionality
yy	Total Number of SRIO Ports (*) 19 = 19 SRIO ports to rear P2-P6 20 = 20 SRIO ports to rear P2-P6 23 = 19 SRIO ports to rear P2-P6 + 4 SRIO ports to front panel 24 = 20 SRIO ports to rear P2-P6 + 4 SRIO ports to front panel or 24 = 24 SRIO ports to rear P1-P6 28 = 24 SRIO ports to rear P1-P6 + 4 SRIO ports to front panel * Not all SRIO ports go to the backplane. May be a combination of backplane & front panel.

Note: Not all possible configurations are offered, consult Curtiss-Wright for available configurations.

Table 5: Recommended Standard Variants

Product Number	Ruggedization	Description
VPX6-6902-A04028 VPX6-6902-A14028	AC L0 AC L100	SRIO data plane switch with 28x SRIO (x4) ports (24 to backplane P1 to P6 and 4 to front panel), OpenVPX profile MOD6-SWH-24F, 0.85" pitch with 1" faceplate
VPX6-6902-C24024	CC L200	SRIO data plane switch with 24x SRIO (x4) ports (24 to backplane P1 to P6), OpenVPX profile MOD6-SWH-24F, 0.85" pitch
VPX6-6902-A04124 VPX6-6902-A14124	AC L0 AC L100	SRIO data plane switch with 24x SRIO (x4) ports (20 to backplane P2 to P6 and 4 to front panel), 16x SerDes GbE to backplane on P1, 2x 1000Base-T to P5/P6, OpenVPX profile MOD6-SWH-16U20F, 2x 10 GbE + 1x 1000Base-T to front panel, 0.85" pitch with 1" faceplate
VPX6-6902-C24120	CC L200	SRIO data plane switch with 20x SRIO (x4) ports (20 to backplane P2 to P6), 16x SerDes GbE to backplane on P1, 2x 1000Base-T to P5/P6, OpenVPX profile MOD6-SWH-16U20F, 0.85" pitch
VPX6-6902-A04123 VPX6-6902-A14123	AC L0 AC L100	SRIO data plane switch with 23x SRIO (x4) ports (19 to backplane P2 to P6 and 4 to front panel), 20x SerDes GbE to backplane on P1/P2, 2x 1000Base-T to P5/P6, OpenVPX profile MOD6-SWH-20U19F, 2x 10 GbE + 1x 1000Base-T to front panel, 0.85" pitch with 1" faceplate
VPX6-6902-C24119	CC L200	SRIO data plane switch with 19x SRIO (x4) ports (19 to backplane P2 to P6), 20x SerDes GbE to backplane on P1/P2, 2x 1000Base-T to P5/P6, OpenVPX profile MOD6-SWH-20U19F, 0.85" pitch



Warranty

This product has a one year warranty.

Contact Information

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