Data Sheet

VPX3-450

Xilinx® Virtex®5 based 3U VITA-46/48 Module

Features

- One user-programmable Xilinx® Virtex®-5 FPGA node (LX155T or SX95T) with:
  - One bank of 275 MHz DDR2 SDRAM (256 MB), up to 2.2 Gbytes/s peak bandwidth
  - Two banks of 275 MHz QDR SRAM (18 MB total), up to 4.4 GBytes/s peak bandwidth
  - Two 4-lane 3.125 GHz serial links to the backplane
  - One 4-lane PCI Express® (PCIe) link to the onboard switching fabric
  - 18 pairs (36 pins) of discrete LVDS signals to the backplane
- One Dual-core Freescale Power Architecture™ MPC8640 PowerPC
  - Running at 1 GHz
  - Up to 1 GB of DDR2 with ECC
  - 256 MB of flash with write protection for user code, data, or FPGA bitstreams
  - Protected backup flash
  - Two Gigabit Ethernet interfaces, factory configurable to either 1000Base-T or 1000Base-X
  - Two EIA-232 serial ports, one can be alternatively configured as EIA-422
  - Connections to the FPGA configuration bus and command/control bus
- Onboard PCIe switch
  - 8-lane port to the MPC8640 processor node
  - 4-lane port to the FPGA node
  - 8-lane port to the XMC site
  - Two 4-lane ports to the backplane, one is factory-configurable to be Serial RapidIO® (sRIO)
- XMC site
- Thermal sensors for monitoring board temperatures
- Support for ChipScope™ Pro and JTAG processor debug interfaces
- Continuum Vector subroutine library available
- VITA 48 1" pitch format
- Multi-board synchronous clock
- Continuum FXtools for the VPX3-450
  - FPGA design kit with highly-optimized IP Blocks, development environment, reference designs, scriptable simulation test benches and software libraries
  - Continuum Firmware and BSP for VxWorks® and Linux® and systems library kit for the MPC8640 processor
- Range of air- and conduction-cooled ruggedization levels available

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Overview

The VPX3-450 is a reconfigurable computing platform designed to tackle demanding DSP tasks such as image processing, radar, data compression, and signal intelligence. Utilizing the massive parallelism and rapid reconfigurability of FPGAs, combined with the flexibility of an AltiVec-enabled dual-core PowerPC™ processor, the VPX3-450 platform is well suited to replace either dedicated ASIC-based hardware or large arrays of processors for front-end signal or image processing, where sustained data rates and processing performance are important to overall system performance, or general algorithm acceleration tasks where data is pushed into the FPGA for calculation performance that may take 10's of general purpose processors to achieve. Many algorithms such as FFTs, 1D and 2D convolutions and filters on incoming data streams may be efficiently implemented in FPGAs. FPGA technology allows unequaled parallelism and enables pipeline processing, typical in DSP applications. Benefits include overall slot reduction, increased processing density and system cost reduction.

The VPX3-450 provides a balanced mix of mezzanine interfaces, high-bandwidth I/O, a variety of high-performance FPGA memories, off-board fabric connectivity with FPGA and general-purpose processing resources. The 3U VPX REDI board features a Xilinx Virtex-5 LXT or SXT platform FPGA (SX95T or LX155T) for user-defined functionality, as well as a Freescale Power Architecture MPC8640D dual-core PowerPC processor node. The board architecture provides a flexible standalone or system level platform for solving a variety of signal processing challenges. Variants of the VPX3-450 are designed to operate in either commercial or rugged environments and are available in air- and conduction-cooled formats.

Thermal management is a critical factor when building high-performance embedded systems. The VPX3-450 provides the ability to monitor the FPGA die and board temperatures as well APIs to set alerts to interrupt an application if temperature envelopes are exceeded.

The VPX3-450 supports a flexible FPGA configuration manager. This allows the designer to store multiple FPGA configuration files in flash or main processor memory. The ability to store configuration files in volatile memory is useful for fast FPGA reconfiguration and storage of classified data or algorithms. The FPGA is easily reconfigured with alternate configuration files via commands from the onboard PowerPC node.

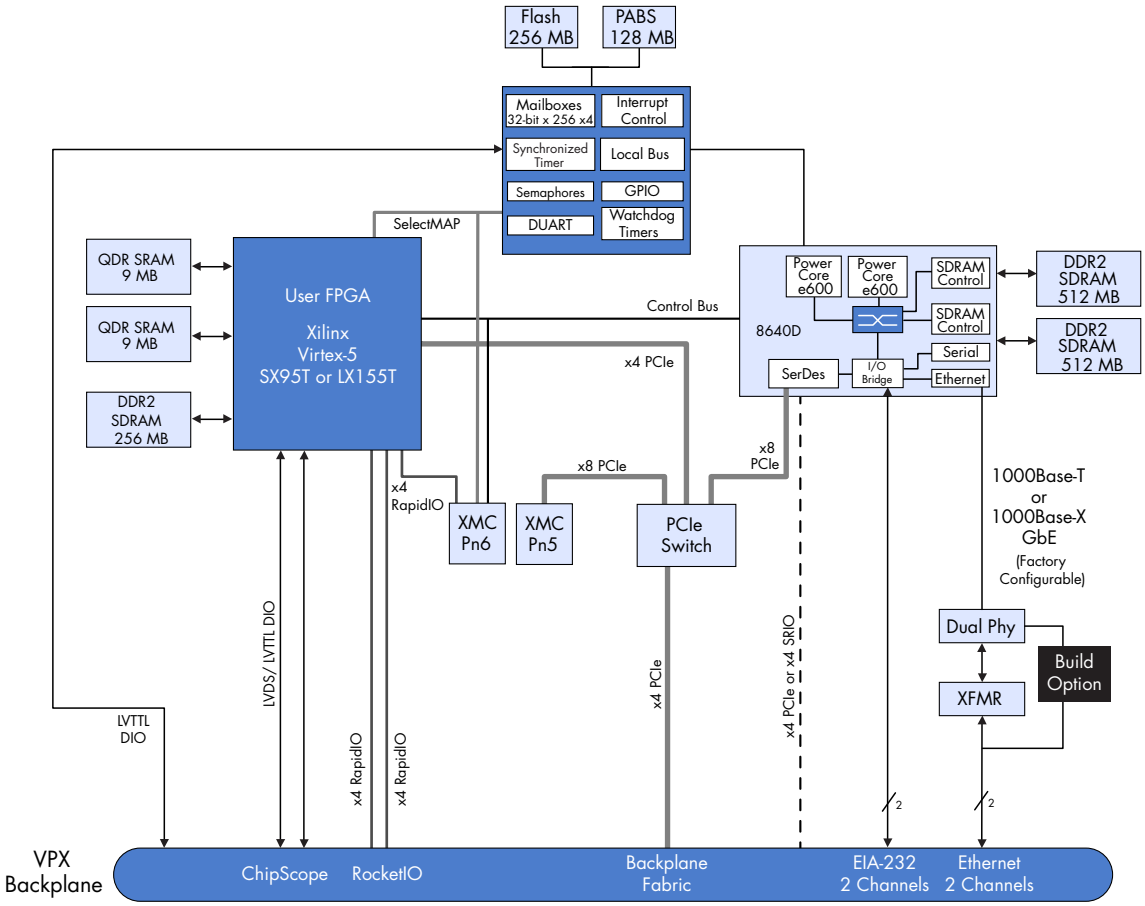
The Continuum FXtools design kit provides a rich set of PowerPC and FPGA-based functions enabling rapid prototyping and deployment of FPGA-based systems. In addition to the full Continuum Firmware and BSP package for the PowerPC, FXtools contains a library of highly-optimized VHDL IP blocks including dual-port memory controllers, PCIe core wrapper, scalable switching interconnect, and advanced DMA engines. Based on the Xilinx ISE™/EDK design flows these blocks can be combined with other off-the-shelf or custom IP blocks to rapidly implement complex, system-on-chip designs. To support this, FXtools includes a set of design templates and example designs, as well as a SystemVerilog (IEEE 1800) simulation testbench with a full set of bus functional models and scripting capabilities. The VPX3-450 provides a JTAG header to support the use of Xilinx ChipScope Pro and JTAG development tools. Refer to the Continuum FXtools datasheet for more details.

Operational Modes

Depending on system processing requirements, the VPX3-450 may be used alone or in conjunction with other system elements. The VPX3-450 supports the following modes of operation:

- Standalone: Does not require other boards in the system for initialization, configuration, development or deployment. The onboard PowerPC node executes code from flash memory and performs all board-level control and status functions.
- System implementation: The board is combined with other VPX boards such as the VPX3-127 single board computer (SBC), VPX3-215 mezzanine carrier, or FPE320 FPGA-based FMC carrier. The onboard PowerPC becomes a peer-computing resource to these other processor-based boards and the FPGAs become computing resources accessible from other processor or FPGA nodes within the system.

Figure 1: VPX3-450 Architecture



Architecture

The VPX3-450 architecture (seen in Figure 1) is suited to DSP applications that place a high premium on sustained I/O throughput, FPGA memory bandwidth and off-board fabric connectivity through either the XMC mezzanine port, rear-panel serial ports, or the PCIe fabric ports. The flexible data flow capabilities of the VPX3-450 ensure that applications can extract the most from the raw computing performance of the Virtex-5 FPGA. The VPX3-450 architecture encompasses a number of key attributes that contribute to maximizing DSP performance:

- A Virtex-5 LX155T or SX95T FPGA and a dual-core MPC8640D PowerPC
- Two high-speed PCIe fabric ports to connect the processing and I/O elements of the VPX3-450 with neighboring hardware in the system
- High-speed serial connectivity (RocketIO™) between the FPGAs, to the backplane, and to the XMC Mezzanine site – up to 1.25 GBytes/s per link
- 6.6 GBytes/s peak memory bandwidth from the FPGA
- Out-of-band control bus for FPGA application command and control

Virtex-5 LXT Details

There are two types of Virtex-5 devices available on the VPX3-450. The LX155T component is a logic-centric device and is the largest gate count component in this Virtex-5 package size. It offers a high density array of logic cells, XtreamDSP48E™ slices and multiple on-chip memory banks to provide flexible I/O or vector processing. These FPGAs allow Gigabit-level connectivity for high-bandwidth, low-latency FPGA communication. The SX95T, on the other hand, is a DSP processing engine with 5 times the number of DSP48E blocks than the LX155T giving maximum calculation resources for tough DSP processing problems.

Table 1 highlights the Virtex-5 LX155T and SX95T capabilities found on the VPX3-450.

Table 1: Virtex-5 LXT capabilities found in the VPX3-450

Capability		LX155T	SX95T
Logic Resources	Slices	24,320	14,720
	Logic Cells	155,648	94,208
	CLB Flip-Flops	97,280	58,880
Memory Resources	Max Dist. RAM (kbits)	1,640	1,520
	Block RAM/FIFO w/ECC (36 kbits each)	212	244
	Total BRAM (kbits)	7,632	8,784
Clock Resources	Digital Clock Manager (DCM)	12	12
	Phase Locked Loop (PLL)/PMCD	6	6
Embedded Hard IP Resources	DSP48E™ slices	128	1
	PCIe Endpoint Blocks	640	1

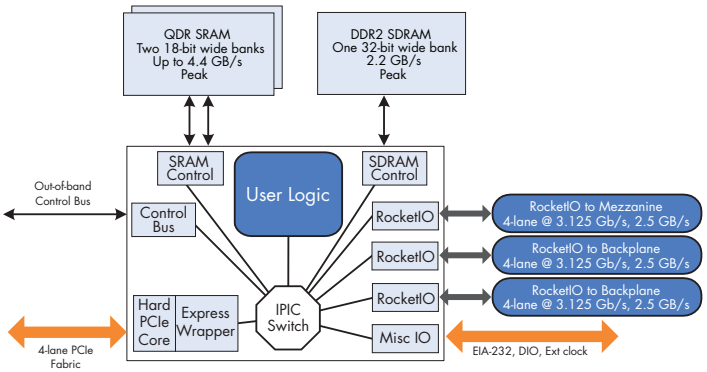
The Virtex-5 offers a number of features that are either enhancements over earlier generation Virtex components or are entirely new to the Virtex-5. The 65 nm ExpressFabric™ logic gate technology of the Virtex-5 is the first to use a 6-input LUT which enables more logic to be packed into a single logic cell and thereby increase speed and area utilization. The Distributed RAM is a 256-bit memory per CLB with 64-bits per LUT, while the Block RAM has been increased to 36 Kbit dual-port blocks with independent clocking on each port. The BRAM memories can be easily configured as single-port, dual-port, or FIFO memory structures and are instrumental in achieving high performance in DSP applications. The DSP48E slices have been enhanced with a 25x18 multiplier and a 48-bit adder to enable single-precision floating point math and wide filters with fewer slices. These features are combined with various power-saving features to make the Virtex-5 an ideal choice for high-performance embedded computing.

User FPGA Architecture

Each user FPGA has a variety of external I/O and memory interfaces as shown in Figure 2. Some or all of the following interfaces may be implemented in a user FPGA design:

- Up to two independent QDR interfaces
- One DDR2 interface
- Up to three off-chip, 4-lane RocketIO interfaces using Aurora™ protocol
- PCIe endpoint with an advanced DMA engine
- Control bus interface
- Switching interconnect

Figure 2: External I/O and Memory Interfaces



Example VPX3-450 Architecture for Xilinx Virtex-5 LX155T or SX95T

(block size not to scale)

DDR2

The FPGA node provides one 256 MByte, 32-bit bank of DDR2 running at 275 MHz. The instantaneous peak data transfer rate to the pair of banks is 2.2 GBytes/s. The DDR2 is intended for temporary data storage, historical data storage, or as a scroll buffer. The DDR2 controller IP block is structured as a dual-port interface to facilitate pipeline designs that have dedicated read and write port structure.

QDR

The FPGA node also provides two 9 MByte, 36-bit banks of QDR for a total of 18 MBytes. The instantaneous peak data transfer rate of these memories is 8.8 GBytes/s. The QDR interface may be implemented as two independent 36-bit interfaces, or a single 72-bit interface. The QDR is intended for temporary data storage associated with DSP algorithms like FFTs or filters. The QDR controller IP block is structured as a dual-port interface to facilitate pipeline designs that have dedicated read and write port structure.

PCI Express Fabric

The VPX3-450 utilizes PCIe interconnect to provide high-speed processor to processor communications both on- and off-board. An onboard switch ties one of the native high-speed ports of the MPC8640 to the XMC site, the Virtex-5 RocketIO GTP transceivers of the FPGA node, and one of the two off-board fabric ports. The second port on the MPC8640 goes directly to the second off-board fabric port. This allows the VPX3-450 to provide both flexible onboard connectivity with high-speed links to neighboring hardware. The 4-lane links provide a maximum 2 GBytes/s bidirectional while the 8-lane links double that to GBytes/s.

Serial RocketIO Connectivity

Xilinx RocketIO GTP transceivers are used extensively on the VPX3-450. In addition to the connections to the PCIe switching fabric, 4-lane GTP ports are used to connect the FPGA node to the mezzanine site, and two 4-lane links to the backplane. These connections allow for a variety of serial interconnect technologies to be used for on- and off-board connectivity such as Xilinx Aurora, XAUI, PCIe or sRIO. Configured as bi-directional, 4-lane links, these paths provide low latency, high performance FPGA or sensor interconnects. All links may operate up to 3.12GHz. (bi-directional bandwidth 2.Gbytes/s). These links can also be controlled using a SW programmable clock device.

XMC (VITA 42)

The VPX3-450 is equipped with one XMC (VITA 42) mezzanine site. The primary interface is switched to allow an 8-lane PCIe (VITA 42.3) connection from the MPC8640 processor capable of 2 Gbyte/s of bidirectional bandwidth, and a 4-lane connection to both the FPGA node and the off-board fabric link capable of 1 Gbyte/s. Additional connectivity to the FPGA node on the VPX3-450 is provided by 8 GTP lanes providing up to 5 Gbytes/s of bidirectional bandwidth.

The conduction-cooled versions of the VPX3-450 adhere to the IEEE 1386-2001and ANSI/VITA 20 standard for conduction-cooled PMCs. The VPX3-450 thermal frame provides the best possible thermal interface for mezzanine modules by supporting the primary and secondary thermal interfaces as defined by ANSI/VITA-20. To support high power XMC modules, the VPX3-450 thermal frame supports a mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed XMC modules can significantly lower the temperature rise between the VPX3-450 card edge and the XMC components. The mid-plane thermal shunt does not impinge on the IEEE 1386-2001 specified component height.

SelectMAP & Command Bus

The VPX3-450 includes two additional communication paths that are not found on Curtiss-Wright's PowerPC-based VPX products. The SelectMAP interface is a set of connections from the PowerPC node utility FPGA used for configuring the user FPGA. The command bus is an additional out-of band communications bus that connects the PowerPC to the user FPGA node. The command bus is used primarily to give command and control instructions to the application running on the user FPGA without interfering with data movements in or out of the primary PCIe interface.

LVDS Discrete Digital I/O

The user FPGA provides thirty-six general purpose LVCMOS25/LVDS25 I/O lines (or 18 LVDS pairs) which are accessible at the backplane connector. Three of these pairs may be used as differential clocks. Each bit is individually programmable to be an input, output or I/O. All bits configured as an input may be used to trigger an interrupt which is further programmable to be level or edge sensitive. Both levels and transition directions may be detected.

Control Node Architecture

The control node on the VPX3-450 is an AltiVec-enabled Freescale Power Architecture MPC8640D dual-core PowerPC processor running at 1 GHz. The MPC8640D provides in a single package two e600 cores, dual-DDR2 memory controllers with ECC, a sRIO interface, a PCIe interface, Gigabit Ethernet controllers and serial I/O controllers. The e600 core and AltiVec units of the MPC8640D processor are based on the proven internals of the MPC7448 processor, offering a large 1 MB internal L2

cache. Existing C, assembly and AltiVec assembly code will run on the MPC8640D without change.

Double Data Rate DDR2

Control node on the VPX3-450 supports 1 Gbyte of DDR2 using the dual memory controller feature of the MPC8640 processor, providing a peak memory bandwidth of 6.4 GBytes/s. The memory is protected with Error Checking and Correcting (ECC) circuitry that can detect and correct all single-bit errors and detect all double-bit errors. The high memory bandwidth will support demanding streaming data applications with simultaneous occurrence of dataflow from the processors and PCIe interfaces.

Flash Memory

The VPX3-450 is equipped with 256 MBytes of flash memory. The 32-bit wide interface supports peak transfer rates of 100 MBytes/s to minimize boot and program loading times. For absolute security against inadvertent flash programming or corruption, a hardware jumper is provided to disable write access to the flash.

Permanent Alternate Boot Site (PABS)

The VPX3-450 has a secondary flash subsystem, PABS, which provides a backup boot facility. PABS is typically used in two scenarios. The first is recovery from corruption of the primary flash memory. The VPX3-450 can be made to boot from PABS by asserting a control signal on the backplane or via an onboard jumper. Once the PABS resident firmware is booted the main flash can be programmed to re-instate the standard firmware. The second scenario is the support of de-classification requirements. PABS firmware provides de-classification functions that will scrub the contents of main flash. Since the PABS flash is hardware write-protected, the user is ensured that no classified data can be written inadvertently to PABS.

Serial Ports

The VPX3-450 provides two EIA-232 serial ports to the control node processor, one of which can be alternatively configured as EIA-422. Each EIA-232 serial port uses the MPC8640 DUART to support asynchronous communications with one transmit and one receive signal. Both ports are connected to the backplane connector. One serial port allows the use of the DTR signal to automatically detect the connection of a data terminal and can be used to control the boot-up sequence of the card if desired. When the second port is configured to be an EIA-422 differential serial port, it supports asynchronous communications with one transmit and one receive pair. The EIA-232 ports support operation up to 115,200 baud, while the EIA-422 port supports a maximum of 20 Mbaud.

LVTTL Discrete Digital I/O

The control node provides seven general purpose discrete I/O lines which are accessible at the backplane connector. Each bit is individually programmable to be an input, output or I/O. All bits configured as an input may be used to trigger an interrupt which is further programmable to be level or edge sensitive. Both levels and transition directions may be detected.

Utility Features Mailbox, Semaphores, Timers

The VPX3-450 features a number of utility features to facilitate multi-processor software applications. Each processor core has a mailbox interrupt mechanism whereby a processor can interrupt another processor and deliver a 32-bit value. The board provides sixteen hardware semaphore registers which are typically used to coordinate the sharing of hardware resources between multiple tasks. The hardware solution provides a faster alternative to traditional software/memory techniques and avoids the use of shared memory to access the semaphores. In addition to the timer resources within the MPC8640D, the VPX3-450 provides six general purpose 32-bit timers which may optionally cause an interrupt to any core upon rollover and be preset with an interval value.

Avionics Style Watchdog Timer

The VPX3-450 provides a watchdog timer for each of the processor cores. Each watchdog timer is a pre-settable downcounter with a resolution of 1µsec. Time-out periods from 1 to 32 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, a backplane signal can be asserted to disable all watchdog interrupts. The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register.

For increased system integrity, the watchdog can optionally be configured to operate in "Avionics" mode whereby a minimum interval between writes to the watchdog register is also enforced. In other words, writing to the watchdog register too soon or too late causes an exception event.

Multi-board Synchronous Clock

The VPX3-450 includes a special purpose counter which may be synchronized with corresponding counters on other boards in the same system. This common time base allows a developer to time-stamp messages and/or data buffers, with the knowledge that the local time is maintained at the same value by all the boards in the system. The counter can be set to roll-over to a pre-load value and interrupt on rollover. This feature is typically most valuable for debugging and instrumenting multi-board applications code, which can present challenges in coordinating the distribution of data items between processors.

Thermal Management

The VPX3-450 contains temperature sensors that monitor the board and processor temperature. Thermal management is key when dealing with large FPGAs that can consume a significant amount of power. Two sensors are located along each edge of the board, and one sensor per processor (the control node and the user FPGA) is provided. The control node monitors the sensors through an I2C bus. The thermal sensors provide a programmable over-temperature status that is used to illuminate a red LED as well as provide an interrupt to the system. The software API allows the application to poll the board and die temperatures during development and deployment.

Continuum FXtools

Continuum FXtools is the developers kit for the VPX3-450 and includes the following functionality:

- The full Continuum Middleware and BSP package for the PowerPC (VxWorks, contact factory for Linux or other OS availability)
- VPX3-450 Hardware, Software, and Firmware User's Manuals
- High-performance IP block library
- Example reference designs
- SystemVerilog (IEEE 1800) Modelsim® simulation testbench
- Support for Xilinx ISE, EDK, and ChipScope Pro tools

Refer to the Continuum Middleware and BSP and the Continuum FXtools datasheet for more details.

Options

Contact the factory for configuration options.

Specifications

The VPX3-450 is available in a full range of environmental grades starting from commercial air-cooled to extended temperature, rugged, conduction-cooled versions. This allows the customer to select the board to match the environmental requirements of the platform. The tables below show the power, dimensions and weight of the board.

Table 2: FPGA Power

FPGA Complement	Maximum Power			Typical Power		
	12 V	5 V	3.3 V Aux	12 V	5 V	3.3 V Aux
SX95T/LX155T	See Note 1	60 W See Note 2	See Note 1	See Note 1	35-40 W See Note 3	See Note 1

Notes:
1. 12 V and 3.3 V supply are only used if an XMC module is installed and requires those power rails.
2. This assumes that the FPGA is consuming approximately 15 W and the PowerPC is consuming approximately 25 W worst case.
3. The power consumption of the VPX3-450 is highly dependent on the application loaded onto the FPGAs and the PowerPC processor. The above data is given as guidance only.

Table 3: Dimensions and Weight

Option	Dimension	Weight
Air-cooled	Per VITA 48.1	0.745 lbs (0.339 kg)
Conduction-cooled	Per VITA 48.2	1.20 lbs (0.544 kg)

Table 4: Cooling Air Requirements

Configuration	Temperature Range	Air-flow
Dual-core	0° - 50°C	15 CFM
Dual-core	-40° - 71°C	15 CFM

Note:
Air-flow is specified for sea-level conditions. The temperature refers to the inlet temperature at the card. The air-flow specifications are for worst case (highest power) conditions, without an XMC installed. Curtiss-Wright can supply additional recommendations for specific power/temperature/altitude scenarios to support the design and testing of cooling subsystems.



Part Numbers

Check with a Curtiss-Wright representative for availability of specific part numbers.

VPX3 - 450 - U V W X Y Z A

- Build Options: Alpha-numeric
- FPGA Type: 1: SX95T, 3. LX155T
- Processor: 2: Dual-core MPC8640D
- Backplane Interface: A: Standard VPX3
- Mechanical Format: 4: 1" pitch, no 2-level maintenance support, 5: 1" pitch, 2-level maintenance support (covers)
- Temperature Range: 0: 0°C to 50°C, 1: -40°C to 71 °C, 2: -40°C to 85°C
- Cooling Method: A: Air-cooling, C: Conduction-cooling
- Model Number
- Standard Prefix for 3U VPX cards

A formal quote from Curtiss-Wright or authorized representative will provide a complete part number and description of the configuration.

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

Technical Support

For technical support:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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