Data Sheet

PMC-FPGA03

Xilinx® Virtex®-II Pro Processing Engine PMC Module

Applications

The PMC-FPGA03 is designed to solve demanding scalable processing requirements in embedded systems, it is particularly suitable for applications such as:

- Radar / Lidar
- Electronic warfare / Signal Intelligence (ELINT) / Surveillance
- Real-time imaging / Inspection / Machine vision
- Medical imaging

Features

- Xilinx Virtex-II Pro XC2VP50 FPGA
- 4x Front panel serial I/O links operating up to 3.125Gbps or 138 discrete I/O lines
- 64 discrete PMC user I/O (P14) lines
- 2x 64Mbytes DDR SDRAM
- 3x QDR-II SRAM - 2Mx18-bit per bank as standard
- 64-bit, 66MHz Master/Slave PCI interface
- Modular front panel I/O system
- Ruggedized versions available (Air or Conduction cooled)
- Windows 2000/XP, VxWorks and Linux support

Overview

The PMC-FPGA03 is a Xilinx Virtex-II Pro FPGA based PMC module designed for commercial/air-cooled and rugged/conduction-cooled environments where performance counts. To maintain the high performance data throughput needed by many leading-edge signal processing applications, a range of flexible data I/O options are available for the PMC-FPGA03, either through the front panel (via adaptor modules) or through the PMC's user I/O connector.

FPGA

At the heart of the PMC-FPGA03 is a Xilinx Virtex-II Pro XC2VP50 FPGA. This can be used for implementing highly parallelized DSP algorithms that include parallel data I/O (LVDS or single-ended, via a front panel adaptor module) or multi-Gbps serial I/O. The FPGA also has embedded PowerPC 405 CPUs available for use in a developer's applications.

Flexible Digital I/O

Adaptable digital I/O is a major factor in determining how easy it is to integrate a processing element into a systems environment. With this in mind, the PMC-FPGA03 supports a range of digital I/O options including serial communications, analog I/O, LVDS, FPDP and custom interfaces.

Front panel I/O is routed to a 180 way 0.5mm pitch, high bandwidth socket. Of the 138 individual signals routed to the front panel connector, 66 are routed as differential pairs. The FPGA is used to control I/O protocols and

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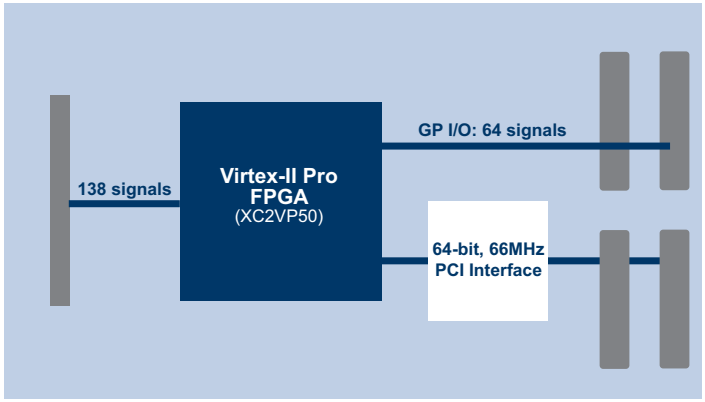
timings. This allows connections to be made through a simple adapter module. 5V, 3.3V and 2.5V power is supplied to the front panel module socket, giving great flexibility to those wishing to design their own modules.

PMC User I/O (P14) has 64 lines available, routed as 32 differential pairs.

The FPGA signals are banked: two banks (69 signals each) are routed to the front panel and another bank (64 signals) is routed to the PMC user I/O connector. Each bank is configurable to 2.5V or 3.3V signaling.

Figure 1: Front Panel I/O Option - Parallel Digital I/O



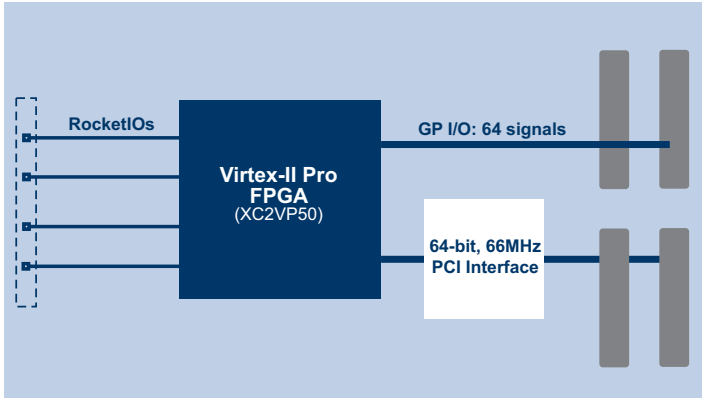
Multi-Gigabit Serial I/O

As an alternative to parallel digital I/O, the PMC-FPGA03 can use high-speed serial communications through the FPGA's RocketIO™ ports, operating at up to 3.125Gbps. The ports are full duplex with each channel having a separate input and output differential pair. The operational speed of the links is determined by an onboard reference oscillator. A range of frequencies are available as build options.

RocketIOs can be used either as low-level data 'pipes' or to implement interfaces such as serial RapidIO or Infiniband using firmware IP cores.

Front panel RocketIO can use up to four High Speed Serial Data Connector 2 (HSSDC2) which are identical to Infiniband 1X connectors. Note: Front panel RocketIO and digital I/O options are mutually exclusive.

Figure 2: Front Panel I/O Option - Rocket I/O



Memory

The PMC-FPGA03 eases algorithm implementation by supplying the designer with two types of high performance external memory: SDRAM for high capacity and SRAM for fast random access.

SDRAM

Two independent banks of 16-bit wide DDR SDRAM, each 64Mbytes, are connected directly to the FPGA and clocked at 125MHz for a peak transfer bandwidth of 500Mbytes/s per bank. As the memory banks are connected directly to the FPGA rather than via a memory bus, there is much greater flexibility in their use: for example, the banks can be used as swing buffers where one bank is filled with incoming data while the second is emptied, using a DMA, to the PCI bus.

QDR SRAM

Three banks of QDR-II SRAM are supplied, each supporting simultaneous read and write operations, clocked at 125MHz. Each QDR memory bank has a separate read and write data bus which is clocked on both the rising and falling edge of the reference clock to provide 500Mbytes/s bandwidth in both directions. Curtiss-Wright supports 1 or 2Mx18-bit banks. The device footprint is capable of taking higher capacity devices as they become available (e.g. 8Mx18-bit). The QDR memory banks are also independently connected directly to the FPGA to provide the developer with maximum flexibility in how the devices may be utilized.

PCI Interface

The PMC-FPGA03 features a 64-bit, 66MHz initiator/target PCI interface through a Quicklogic QL5064 bridge from the 64-bit, 80MHz local bus which interfaces to the FPGA and FLASH memory. The interface supports configuration of the FPGA from a host and includes full FPGA to PCI interrupts and DMA. The PCI core interface has six FIFOs, four DMA engines, mailbox registers and complex interrupt support. Example VHDL code is provided to allow the developer accelerated access to the built-in resources of the PMC module.

Figure 3: PMC-FPGA03 with LVDS-MOD3 differential front panel I/O

Software

A range of software development tools are supplied for the PMC-FPGA03. These include low level VHDL code, drivers, board support utilities, high-level design tools and IP cores.

Board Support Package

Software development is supported by a board support package (BSP) that includes device drivers, a set of host-based utilities, host application libraries, numerous example programs and full source code to the libraries and device drivers.

The host utilities provide a set of tools to help give oversight of the board architecture. This allows for system evaluation, functional testing and configuring of the FPGA. The utility package includes:

bview A monitor program running as a Windows application which provides a complete display of the installed Curtiss-Wright hardware in a system. The display is hierarchical, allowing users to select individual boards within a system for further investigation of lower level hardware; including all Xilinx and interface registers as well as SRAM, SDRAM and FLASH memory.

bviewd A remote monitor for non-Microsoft platforms, such as Linux or VxWorks that accepts remote connection from bview on a Windows host so that bview operates as the graphical user interface for the monitor. bviewd is fully multi-threading and allows connections from multiple bview instances.

pfcfg A FLASH programming and FPGA configuration utility that allows the FPGA to be configured from a file on the host file system or from FLASH.

pfprobe A general purpose system status evaluation tool that is able to probe the system bus for all PMC-FPGA boards. For each card found, it is able to display board information, perform a complete functional test of the board and assess the PCI data transfer bandwidth of the board.

Libraries

The libraries provide integration support and levels of abstraction for using the PMC-FPGA03 from a host application. They are C++ libraries built using Microsoft Visual C++ for Microsoft Windows NT/2000/XP platforms and the GNU compiler for VxWorks and Linux. The main functionality is to provide user programs with access to registers and memory regions while supporting interrupts and DMA engines. Services include:

- Initialization
- Configuring the FPGA
- Host accessing of PMC-FPGA Boards - expose regions to the PCI bus.
- Accessing Flash Memory.
- Allocating DMA Buffers
- Synchronizing Interrupts
- DMA Driven I/O
- FPDP Interface

Example programs which use these library routines for interfacing with example firmware are included to demonstrate tasks such as setting up DMAs, using the DDR SDRAM and QDR-II SRAM and how the board handles interrupts.

Firmware

Library firmware, creating standard interfaces between the FPGA and other board hardware, is supplied in the BSP. This has been developed with Xilinx ISE logic design tools and HDL synthesis has been generated for Xilinx synthesis technology (XST). Curtiss-Wright's manuals guide users on transitioning to other synthesis tools such as Synplicity Synplify.

Firmware designs for a multitude of algorithms are available from many sources, including Curtiss-Wright, in the form of intellectual property (IP) cores. See http://www.Curtiss-Wright.com for more information on available cores.

I/O Modules

The PMC-FPGA03 provides a high degree of I/O flexibility including both front panel and PMC P14 based [user] I/O. Front panel I/O is supported by I/O modules.

See www.cwcembedded.com for information on modules including RS485, LVDS and analog I/O.

Ruggedized versions

Curtiss-Wright offers ruggedized versions of the PMC-FPGA03 that are characterized for extended temperature range, shock, vibration, altitude and humidity. These boards are equipped with extra and/or special hardware to improve tolerance against shock and vibration.

Table 1: Specifications

FPGA	
Device	Xilinx Virtex-II Pro XC2VP50 (Contact Curtiss-Wright for other sizes)
Package	FF1152
Memory	
DDR SDRAM with ECC	2x 64Mbytes @ 125MHz
QDR-II SRAM	3x 2Mx18-bit @ 125MHz
FLASH	4Mbytes
PCI Interface	
Device	Quicklogic QL5064
Compliance	PCI 2.2: 32/64-bit, 33/66MHz 3.3/5V tolerant Initiator/Target/DMA
Enhancements	DMA, Interrupt support
Bandwidth	up to 528 Mbytes/s
Standards	
Compliance	IEEE 1386.1 (PMC Module) specification & ANSI/ VITA 20-2001 conduction cooled PMC

Input / Output	
Front Panel Parallel I/O	138 lines + Power routed to Samtec QSH-00-01-FDA
Front Panel Serial I/O	4x RocketIO to HSSDC 2 up to 3.125Gbps signaling
User I/O (PMC P14)	64 bit data
Software Support	
Firmware Tool Chain	Xilinx ISE 7.x*, XST
Utilities	Board memory viewer Confidence tests Flash and FPGA configuration
Libraries	API for DMA, Interrupt and hardware manipulation
Firmware	Interface & Simulation components

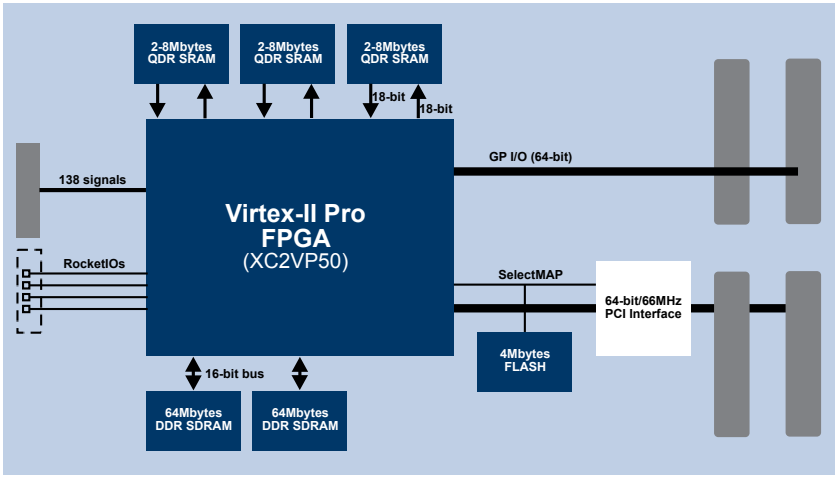
* Contact Curtiss-Wright for the latest supported toolchain

Table 2:
Environmental Specifications

		Air-cooled			Conduction-cooled
		Level 1	Level 2	Level 3	Level 4
Temperature	Operational[1] (at sea level)	0°C to 50°C Inlet 8 cfm air flow	-10°C to 65°C Inlet 8 cfm air flow	-40°C to 75°C Inlet 8 cfm air flow	-40°C to 75°C Card edge temp.
	Non-operational	40°C to +85°C	-40°C to 85°C	-55°C to 85°C	-55°C to 85°C
Vibration	Operational (Sinus)	-	-	10G peak 15-2,000Hz	10G peak 15-2,000Hz
	Operational (Random)	-	0.02 g2/Hz (20-2000Hz)	0.04 g2/Hz (15-2000Hz)	0.1 g2/Hz (15-2000Hz)
Shock	Operational	-	30 g peak 11ms half sine	30 g peak 11ms half sine	40 g peak 11ms half sine
Humidity	Operational	0-95%	0-100%	0-100%	0-100%
Altitude	Operational	10,000ft	20,000 ft	20,000 ft	70,000 ft
Conformal Coat		No	Yes	Yes	Yes

Notes
1. The maximum operating temperature is heavily dependant on the power dissipation of the FPGA devices: Applications with high levels of FPGA utilization may not operate to the maximum ambient temperatures stated.)

Figure 4: PMC-FPGA03 Block Diagram



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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