PMC-E2600

Rugged, High-Speed Digital Transmitter PMC

Dual, Flexible Outputs
- 200Msps 14-bit DACs providing
- Quadrature modulated signals up to 80Mhz Fc, 25MHz bandwidth
- Baseband signals to 22.5MHz
- Single tones up to 80MHz

Low Risk Ruggedisation
- Specifically designed for rugged environments
- Easy translation from commercial prototype to rugged production
- Rugged and commercial variants share the same PCB layout

FPGA Resource for Custom DSP
- 90% of 3 million gate Virtex II accessible
- Firmware development kit available
- Custom design service offered

Comprehensive BIT
- On-board ADCs support testability of both Analog and Digital sub-systems
- Support for PBIT, BBIT & IBIT modes

Multiple DMA Engines
- Maximise use of PCI 2.2 interface
- Capable of supporting continuous waveform generation at the board's maximum data rate

Overview

The PMC-E2600 Digital Transmitter PMC from Curtiss-Wright is the leading solution for transmission of high-speed analog signals in Radar and Software Radio applications.

- Dual, synchronised 200Msps D/A conversion channels, offering multiple up-conversion and analog reconstruction schemes.
- Configurable waveform storage for each transmit channel.
- Substantial FPGAs resources, interconnected to maximize flexibility.
- High-bandwidth transfer over 64-bit 66MHz PCI enabled using powerful on-board DMA engines.
- Two high speed ADCs provided on-board to enable comprehensive BIT.
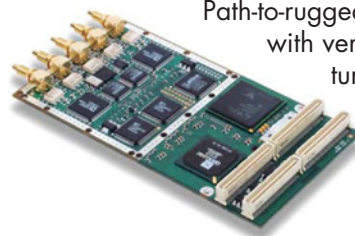
Path-to-rugged design is inherent in the product range, with versions available for extended temperature, shock and vibration and air- and conduction-cooled environments.

For more information on our broad range of high-integrity computing solutions, please visit our website at **www.cwcembedded.com**

## CURTISS WRIGHT Controls

Embedded Computing
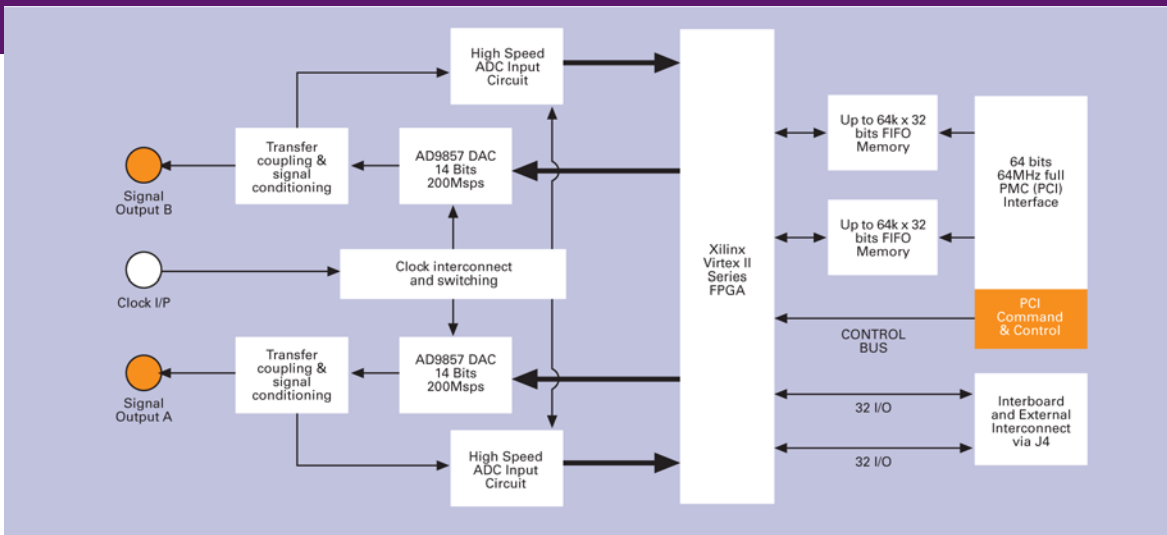
Functional Description

Analog Outputs

The PMC-E2600 has versatile on-board Quadrature Modulating digital-to analog convertors (AD9857) that can be used to produce a variety of analog outputs. Baseband interleaved I and Q data can be up-converted and modulated to produce complex quadrature modulated signals at up to 80MHz. Alternatively single channel 14-bit data can be entered to create base-band signals up to 22.5MHz (over-sampled at up to 200Msps) In both cases the digital to analog convertors' internal filters can be configured to condition the signal prior to re-construction. The FPGA can be programmed to provide extra filtering, encoding, interpolation, pulse shaping, etc as required.

In addition, with the data inputs disabled the convertor's on-board DDS capability can be used to provide single tones at desired frequencies up to 80MHz. The frequency is directly controlled via a 10MHz serial interface and can be used to produce a FSK modulated signal, or test tones for BIT and system calibration.

The analog output signals are AC coupled via transformers to SMC front panel connectors.
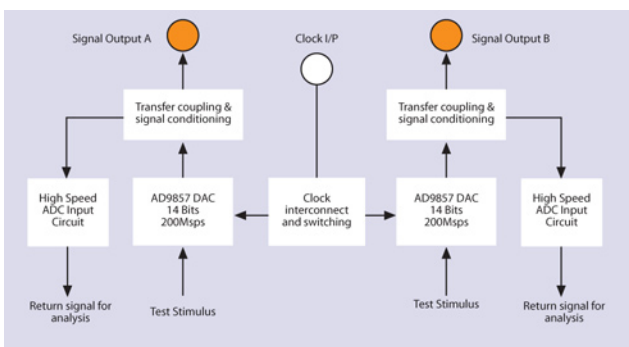
DSP Functionality & Digital Up Conversion

A user-programmable Xilinx Virtex™ II FPGA and the AD9857 Quadrature Digital Upconvertors provide the PMC-E2600 with a powerful suite of prereconstruction DSP capabilities.

For scalability, the PMC-E2600 is available with either an XC2V1000 or XC2V3000. In standard configuration over 70% of a XC2V1000 remains free and can be used for specific DSP functions. For example, the FPGA can be used to pre-condition the data prior to transmission by the modulating DAC. This conditioning could vary from simple filtering of baseband data, up to Grey coding, scrambling, symbol mapping and interleaving of quadrature data for complex QAM signals. In addition, it is possible to use the FPGA for on-board waveform generation; examples are test patterns and tones for system calibration or built-in-test.

Curtiss-Wright have experience in the firmware design of low power, spectrum management algorithms and filtering functions. As a result Curtiss-Wright can tailor the PMC-E2600 FPGA firmware to meet specific application requirements. Alternatively, a Firmware Development Kit (FDK) is available which provides source code for the Interfacing modules, allowing the user to develop proprietary algorithms using third-party tools.

Programmable logic also implements the host control interface using a bank of 32-bit internal registers accessible over the PCI bus.

Data Storage & Host Interfacing

The 64-bit 66MHz PCI interface on the PMC-E2600 provides extremely flexible host communication, with over 500Mbytes/s nominal bandwidth and full interrupt and mailbox functionality. Standard JTAG signals for test chaining and FPGA programming are available. The PMC P4 connector is linked directly to the FPGA for user I/O, which enables inter-board synchronization and custom data interfacing for proprietary buses. The ANSI VITA

35-2000 standard for VME P2 routing to PMC P4 supports this approach to route trigger signals through P4. Each analog channel has its own dedicated bi-directional FIFO buffer with 32-bit width and 64k depth, which equates to 128k samples per input channel and a total of 512kB on-board storage. These FIFO buffers can be synchronized to provide full 64-bit long word transfers over the PCI interface using multiple DMA engines and both interleaved and non-interleaved data transfers. The Bi-FIFOs allow for each channel to be configured as input or output with the FIFO storing either digital output data for output waveform generation, or received pre-processed input data such as returns from the on-board A to D convertors used for built-in-test (BIT).

Support for Testability

Built-in test support is fundamental in the PMC-E2600 product family and extensive facilities are available for Power-Up, Background, Intrusive and Non-Intrusive BIT. For example, two high-speed 14-bit ADC circuits are available to digitize test signals injected into the input signal paths of the DAC. Each ADC output is fed to the opposite signal path to maximize the testability and the presence of a test tone can then be verified by run-time analysis of the returned data stream. The PMC-E2600 is also capable of supporting a boot PROM containing BIT control functions for automatic execution of a configurable set of BIT routines on power-up.

Target Applications

Software Radio

The on-board FPGA resources provide the capability to add user defined, pre-reconstruction signal processing (scrambling, coding, etc). In addition, the quadrature modulators can be configured to produce three signal types:

- Quadrature modulated signals from interleaved I and Q data. These signals can have a bandwidth of up to 25MHz and can be internally upconverted to 80MHz.
- Interpolated baseband signal up to 22.5MHz.
- Single tones up to 80MHz, using the internal DDS, that can be (frequency) modulated at up to 10MHz rate.

Re-programming the FPGA can be achieved using the PMC's standard JTAG interface. The quadrature modulators are fully configurable through the PCI interface. The re-configurable nature of this capability supports the objective of Software Radio and can effectively increase the processing density of the overall system.

Radar

Wide usable bandwidth (80MHz), flexible output signals (single tone or quadrature modulated) and a high SFDR (>80dB @ 65MHz o/p) make the PMC-E2600 transmitter ideal for modern Radar applications.

Companion Products

Designed with a similar system interface, the PMC-E2600 is the ideal companion to Curtiss-Wright' RAD-2 receiver product. Together, these products offer a complete transmit/receive digitization solution for high-performance sensor processing applications.

Environmental Specification

The PMC-E2600 is designed path-to-rugged in accordance with the ANSI/VITA Conduction Cooled PMC specification and accommodates central stiffening bars on the host board. The PMC-E2600 is available at three ruggedization levels (see ordering information for details) including a cost-effective commercial version for prototyping in benign environments.

Software Drivers
- Device drivers are available for Linux and VxWorks
- Full documentation and source code are provided
- All software is supported directly by Curtiss-Wright

Example QAM Operation
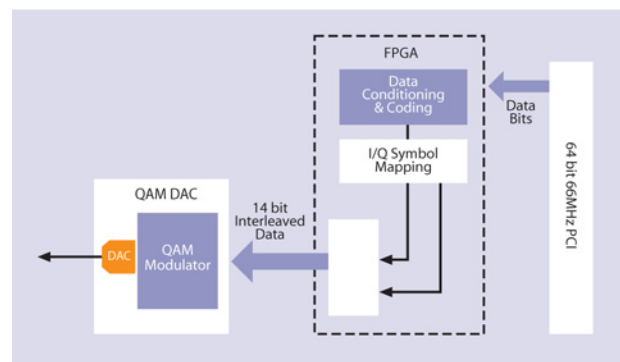
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Specifications

Analog Output

- Channel Count   2 simultaneous
- Resolution   14-bit
- Clock Rate   Up to 200 MHz
- Output Frequency   1 to 80MHz
- Output Signal   ± 0.25V (AC coupled) into 50 ohm
- SFDR   > 80dBc @ 65MHz
- Phase Noise   145dBc/Hz @ 1kHz offset

Clock Input

- Clock Input Format   ± 1V, AC coupled
- Clock Input Threshold   zero crossing
- Clock Input Impedance   50Ω
- Clock Connector   SMC via Front Panel
- Clock Frequency   10 to 200 MHz

Trigger Input

- Selection   Factory Configurable
- via PMC J4   TTL level, 10kΩ impedance
                         LVDS, 100Ω termination (connected to FPGA)

Digital Subsystem

- PCI Interface   64-bit/66MHz rev 2.2 compliant
- User FPGA   Xilinx Virtex II XC2V Series

Physical & Environmental Specifications

- Single Width PMC Module, IEEE 1386.1 compliant Commercial, Extended Temperature, Air Cooled and Conduction-Cooled versions available

Contact Curtiss-Wright for Definition of EnvironmentalSpecifications Information Sheet.

Firmware Development Kit (FDK)

The PMC-E2600 FDK includes VHDL modules for interfacing the DACs, BiFIFOs and Local Bus to the Xilinx FPGA. Please contact Pentland directly for further details and ordering information.

Software Support

Device drivers available for VxWorks & Linux Operating Systems.

Please contact Curtiss-Wright directly for further details and ordering information.

Ordering Information

PMC - E2600 - CT0002zz

Part Number	Description
C	cooling - air or conduction-cooled (A/C)
T	temperature range - 0=L0, 1=L100
00	# input channels
02	# output channels
zz	product specific variants

Please contact Curtiss-Wright directly for further details and ordering information.

www.cwcembedded.com