Product Fact Sheet

PMC-E2200

Rugged, High-Speed Digital Receiver PMC

Dual channel 105 Msps 14 bit A to D Conversion
- Wide bandwidth (>200MHz)
- High SNR (> 12 ENoBs)
- Good spectral purity
- SINAD > 72dB
- THD > 82 dB

Low Risk Ruggedization
- Specifically designed for rugged environments
- Easy translation from commercial prototype to rugged production
- Rugged and commercial variants share the same PCB layout

FPGA Resource for Custom DSP
- 90% of 3 million gate Virtex II accessible
- Firmware development kit available
- Custom design service offered

Clock De-skew Circuits
- Removes phase error in the analog domain.
- Corrects cable mismatch, quadrature imbalance etc.
- Available on synchronous or independent clocks

Comprehensive BIT
- On-board DACs support testability of both Analog and Digital sub-systems
- Support for PBIT, BBIT & IBIT modes

Multiple DMA Engines
- Maximize use of PCI 2.2 interface.
- Capable of supporting continuous capture at the board's maximum 420MB/s.

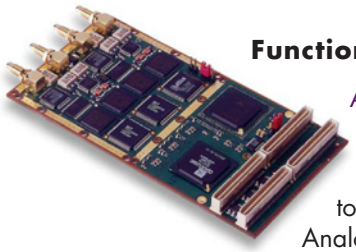
For more information on our broad range of high-integrity computing solutions, please visit our website at **www.cwcembedded.com**

Overview

The PMC-E2200 Digital Receiver PMC from Curtiss-Wright is the leading solution for acquisition of high-speed analog signals in Radar, Software Radio and Signal Intelligence applications.

Dual 105Msps analog acquisition channels are augmented by substantial FPGA resources and up to 16 individual down-conversion channels provided by 4 GC4016 down convertors. High-bandwidth transfer over 64-bit 66MHz PCI is enabled using powerful on-board DMA engines. Extensive support for system-level functionality such as built-in test is also provided. OS Drivers are available for VxWorks and Linux.

Path-to-rugged design is inherent in the product range, with versions available for extended temperature, shock and vibration and air- and conduction-cooled environments.



Functional Description

Analog Acquisition Subsystem

The high-speed analog interface features two ADC channels, each sampling at up to 105Msps with 14-bits resolution, using the Analog Devices AD6645 convertor. The inputs are AC-coupled via RF transformers and provides bandwidth in excess of 200 MHz. The PMC-E2200 allows direct undersampling of frequencies throughout the VHF spectrum. Input channels can be sampled independently from two external clock sources using individual clock circuits, or alternatively, the channels can share the same clock if synchronized sampling is required. Two high-speed 14-bit DAC circuits have been incorporated for offset correction and dithering techniques, and to enable comprehensive built-in test.

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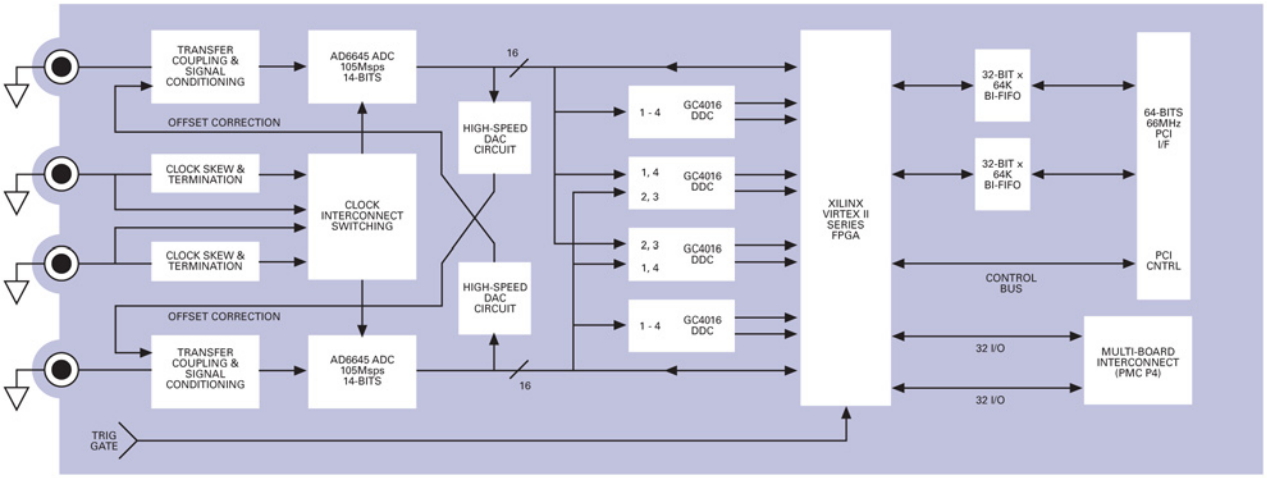


Another unique feature of the PMC-E2200 is the clock de-skewing capability for alignment of in-phase & quadrature (IQ) sampling points, thereby compensating for delays in the receiver chain. This facility allows removal of analog path length delays in multi-element phased array applications. When fitted, the delay is controlled by a 10-bit digital value and has a minimum of 1.2ns and a maximum of 12.2ns, giving a delay step resolution of 10ps.

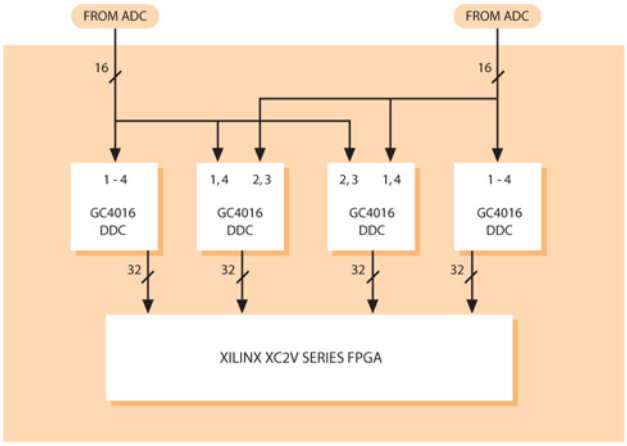
Digital Down Conversion & DSP Functionality

The PMC-E2200 has a powerful suite of post-acquisition DSP capabilities, with a user-programmable Xilinx Virtex™ II FPGA and up to 4 Graychip 4016 Quad Digital Down-Convertors.

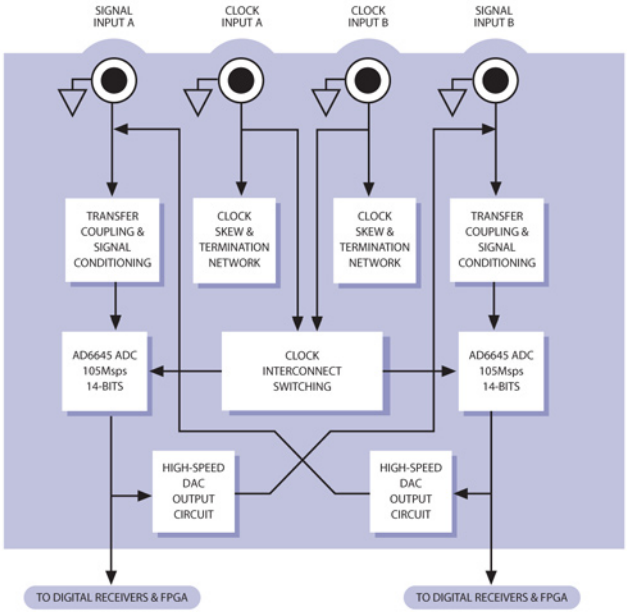
Programmable logic implements the host control interface using a bank of 32-bit internal registers accessible over the PCI bus. For scalability, the PMC-E2200 is available with an XC2V1000 or XC2V3000. Over 90% of a XC2V3000 remains free and can be used for specific DSP functions. Curtiss-Wright is experienced in the firmware design of many spectrum management algorithms and filtering functions with lowpower dissipation and can tailor the PMC-E2200 to meet specific application requirements. Alternatively, a Firmware Development Kit will be available that provides source code for the Interfacing modules and allows the user to develop proprietary algorithms using third-party tools.

Problems of noise generation and settling time in switching ADCs on and off during acquisition are avoided by running the ADCs continuously. The trigger input can be either via the front panel or the PMC P4 I/F, and is factory configurable. In both cases, it is fed straight to the FPGA where it can be used to control the capture of valid data.

ADC to Graychip Connectivity



Analogue Acquisition Subsystem



Each Graychip DDC has four identical down-conversion circuits, each supporting IQ signal generation, decimation between 8 and 4,096 and flexible control of channel spectral response. Finally, a resampler can combine the four individual channels and adjust the sample rate up or down as required. Each circuit accepts a real sample rate of up to 100MHz and input channels can be combined to increase the input bandwidth and to process complex input data. The maximum single channel output bandwidth is just under 2MHz, and multiple output channels can be combined to increase output bandwidth. In the PMC-E2200, the two ADC outputs are connected to the DDCs as shown in the figure at the right. This configuration provides maximum flexibility in the down-conversion of received signals, allowing Narrowband, Double Bandwidth and Wideband modes of reception.

Input complex data for the DDCs can be generated either by simultaneous sampling of IQ analog signals, or by automatically generating complex data in the ADCs using skewed clocks i.e. combining the sampling and IQ mixing functions. Sample-by-sample skew values can be used to achieve phase manipulation in the sampling.

Alternatively, ADC-generated data can bypass the Graychips and feed directly to the FPGA.

Data Storage & Host Interfacing

The 64-bit 66MHz PCI interface on the PMC-E2200 provides extremely flexible host communication, with over 500Mbytes/s nominal bandwidth and full interrupt and mailbox functionality. Standard JTAG signals for test chaining and FPGA programming are available. The PMC P4 connector is linked directly to the FPGA for user I/O, which enables inter-board synchronization and custom data interfacing for proprietary buses. The ANSI VITA 35-2000 standard for VME P2 routing to PMC P4 supports this approach to route trigger signals through P4.

Each analog channel has its own dedicated bi-directional FIFO buffer with 32-bit width and 64k depth, which equates to 128k samples per input channel and a total of 512kB on-board storage. These FIFO buffers provide full 64-bit long word transfers over the PCI interface using multiple DMA engines and both interleaved and non-interleaved data transfers. These DMA engines may be dedicated to a specific input channel or, alternatively, be linked together to provide an extremely powerful chain DMA capability. The Bi-FIFOs allow for each channel to be configured as input or output with the FIFO storing either received and pre-processed input data or digital output data for output waveform generation.

Support for Testability

Built-in test support is fundamental in the PMC-E2200 product family and extensive facilities are available for Power-Up, Background, Non-Intrusive and Intrusive BIT. For example, two high-speed 14-bit DAC circuits are available to generate test signals for injection into the input signal paths. Each DAC output is fed to the opposite signal path to maximize the testability and the presence of a test tone can then be verified by run-time analysis of the input data stream.

The PMC-E2200 is also capable of supporting a boot PROM containing BIT control functions for automatic execution of a configurable set of BIT routines on power-up.

Target Applications

The PMC-E2200 is purposefully designed for the Radar, Software Radio and Signal Intelligence markets. Unique functionality such as clock deskewing is aimed at relieving the problems encountered in the design of complex, multiple receiving element Radar. In-system reconfigurable down-conversion and filtering functionality supports the objective of Software Radio. With post-acquisition DSP, the PMC-E2200 effectively increases the processing density of the overall system.

The PMC-E2200 is designed path-to-rugged in accordance with the ANSI/VITA Conduction Cooled PMC specification and accommodates central stiffening bars on the host board. Typical power dissipation with an XC2V1000 FPGA executing projected algorithms is 7W. A cost-effective commercial specification version of the PMC-E2200 is available for prototyping in benign environments.

Applications

- Software Radio
  - Multiple-channel, fully reconfigurable digital receiver
  - Digital down-conversion from VHF carrier or IF signal
  - Innovative digital filtering capability
- Radar
  - Wideband, high-resolution, high dynamic range digital
  - Radar receiver
  - Channel-matching & clock de-skewing for Phased Array antennas
  - Low-latency acquisition and front-end DSP for advanced applications
  - Extensive testability and support for BIT & PM
  - Conduction-cooled specification for harsh operating environments
- Signal Intelligence
  - Wideband front-end for direct reception of signals up to 300MHz
  - High-speed, high-resolution A/D conversion
  - Reconfigurable processing resources for specialized functions

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Software Drivers

Device drivers are available for Linux and VxWorks
Full documentation and source code are provided
All software is supported directly by Curtiss-Wright

Specifications

Analog Input

- Channel Count: 2, simultaneous/independent
- Resolution: 14-bit
- Sample Rate: Up to 105Msps / channel
- Input Bandwidth: >200MHz
- Input Ranges: ± 1.0V single-ended
- Input Impedance: 50Ω or 75Ω, factory configurable
- Aperture Uncertainty: 1ps max., typically 0.3ps
- SINAD: > 72dB
- SNR: > 72dB
- THD: > 82dB
- Protection: Maximum input range without damage is ± 5V
- Input Connector: SMC

Clock Inputs

- Clock Input Format: ± 1V, AC coupled
- Clock Input Threshold: zero crossing
- Clock Input Impedance: 50Ω
- Clock Skew Control: ± 0.1%
- Clock Connector: SMC via Front Panel

Trigger Input

- Selection: Factory Configurable
- via PMC J4: TTL level, 10kΩ impedance, factory configurable LVDS, 100Ω termination (connected to FPGA), factory configurable
- via Front Panel: TTL level, 10kΩ impedance

Digital Subsystem

- PCI Interface: 64-bit/66MHz rev 2.2 compliant
- User FPGA: Xilinx Virtex II XC2V Series
- Digital Down Converter: Graychip GC4016

Physical & Environmental Specifications

- Single Width PMC Module, IEEE 1386.1 compliant
- Typical Power Consumption is 7W
- Commercial, Extended Temperature, Air Cooled and Conduction-Cooled versions available

Contact Curtiss-Wright for Definition of Environmental Specifications Information Sheet.

Firmware Development Kit (FDK)

The PMC-E2200 FDK includes VHDL modules for interfacing the ADCs, DDCs, BiFIFOs and Local Bus to the Xilinx FPGA. Options to include DSP functions are also available. Please contact Curtiss-Wright directly for further details and ordering information.

Software Support

Device drivers are available for VxWorks & Linux Operating Systems.

Ordering Information

PMC - E2200 - CT0200zz		
Part Number	Description	
C	Cooling - Air or Conduction-Cooled (A/C)	
T	Temperature Range	0 = L0
		1 = L100
02	# Input Channels	
00	# Output Channels	
zz	Product Specific Variants	

Please contact Curtiss-Wright directly for further details and ordering information.

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