



Data Sheet

MM-6165D

2 or 4GB SDRAM 64-bit
66MHz PMC Module

Features

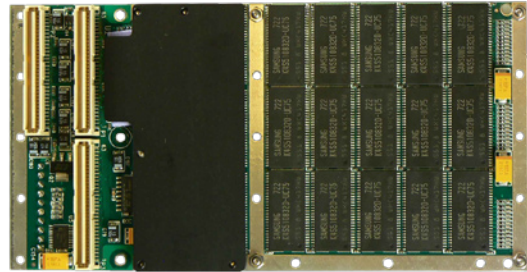
- ◆ Capacity: 2 or 4GB
- ◆ 64-bit 66MHz PCI Interface
- ◆ Up to 533MB/s transfer rate
- ◆ Semaphore Mailbox DMA Engine
- ◆ Error Detection and Correction
- ◆ Supports interrupts
- ◆ Multiple device drivers available

Memory Controller

The MM-6165D controller has a rev. 2.3 compliant PCI interface and operates in both 64-bit and 32-bit PCI modes at 33MHz or 66MHz and is capable of burst mode accesses at the full bus bandwidth at 66MHz. The peak transfer rate is 533MB/s. A sustained transfer rate of 480MB/s is due to refresh overhead. In addition to handling data management, the controller corrects single bit errors and provides double bit detection.

Mailbox DMA

The DMA has been optimized for multi-threaded operating systems and cluster implementations. Instead of just generating an interrupt after a transfer, the DMA writes a semaphore to the host in host memory when the transfer is complete so the host does not have to pole the status of the DMA.



Memory Array

The array utilizes SDRAM devices of differing densities to provide 2 or 4GB of memory.

System Application

PMC's have become the standard form factor of choice for mezzanine cards on today's high performance board level VME and CompactPCI (cPCI) cards. PMC's are electrically equivalent to the traditional PCI bus, and most VME and cPCI single board computers now include one and often two PMC sites for flexible integration.

The MM-6165D can easily provide buffer expansion memory on cards with PMC sites. Memory on the PCI bus is mapped into I/O space, which easily creates a separate and distinct memory partition for buffering data, caching data, or storing application files.

Learn More

Web / sales.cwembedded.com

Email / sales@curtisswright.com

**CURTISS
WRIGHT** Controls
Embedded Computing

Innovation In Motion.
cwembedded.com



Table 1: Specifications

Capacity	2 or 4GB	
Data Integrity	Error detection and correction for all single-bit errors and detection for double-bit errors	
Address	64 bits multiplexed with data on the PMC bus - dual address	
Data In/Data Out	64 bits bi-directional controlled by byte enable signals C/BE[7..0]#	
Compatibility	Common Mezzanine Card Family: CMC, IEEE P1386, Draft 2.2 Physical & Environmental Layers for PCI Mezzanine Cards: PMC, IEEE P1386.1, Draft 2.3	
Burst Mode Transfer Rate	Up to 533MB/s (not including refresh)	
Bus Mastering	DMA Initiator & Target capabilities	
Interrupts	Supports Interrupts	
Refresh	Refresh cycles are 90nsec, every 15.6usec	
Interface	PCI bus compatible Rev 2.2	
Power Requirements (3.3V Supply)	Standby: 325ma Operate: 1.275A	
Power Consumption	3.3V @ 2.2A (worst case)	
Power Dissipation	7.26W (worst case)	
Operating Temperature	D Version: -20°C to +60°C DR Version: -25°C to +65°C	DT* Version: -40°C to +71°C DTE/xGP2* Version: -40°C to +85°C
Storage Temperature	-40°C - +85°C	
Relative Humidity	Up to 95% without condensation	
Vibration	D Version: N/A DR Version: 0.04 g2/Hz based on 15-2kHz, 1hr/ axis sine: 10g peak 15-2kHz, 1hr/axis	DT* & DTE/xGP2* Versions: 0.1 g2/Hz based on 15-2kHz, 1hr/axis sine: 10g peak 15-2kHz, 1hr/axis
Shock	D Version: -N/A DR Version: 30g peak, half sine 11ms	DT & DTE/xGP2 Versions: 40g peak, half sine 11ms
Physical Dimensions	Height: TBD Depth: TBD Front Panel Height: TBD	Width: TBD Maximum Component Height: TBD Weight: .TBD
Safety	All printed wiring boards (PWBs) are manufactured with a flammability rating of 94V0 by UL recognized manufacturers.	
Notes	*DTx versions only available for P2 PMC placement Note: x denotes memory configuration	

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwembedded.com/sales

Email: sales@cwembedded.com

For technical support, please visit:

Website: www.cwembedded.com/support1

Email: support1@cwembedded.com

Warranty

This product has a one year warranty.

The information in this document is subject to change without notice and should not be construed as a commitment by Curtiss-Wright Controls Inc., Embedded Computing (CWCEC) group. While reasonable precautions have been taken, CWCEC assumes no responsibility for any errors that may appear in this document. All products shown or mentioned are trademarks or registered trademarks of their respective owners.