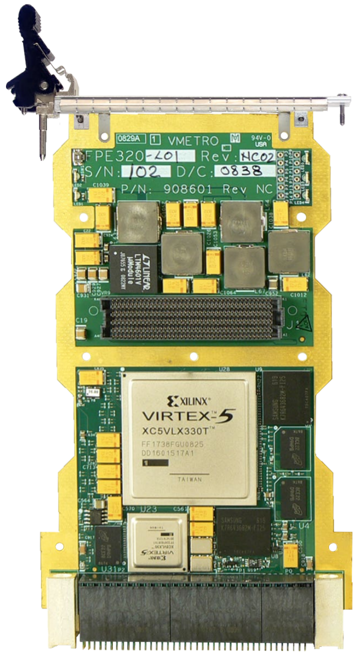
Data Sheet

FPE320

Xilinx® Virtex®-5 3U VPX Processor with FMC Site



Applications

- Electronic Warfare & Signal Intelligence (SIGINT)
- Electronic Counter Measures
- UAV Sensor Acquisition
- Semiconductor Inspection
- Seismic Imaging

Features

- Supports Xilinx Virtex-5 SXT and LXT FPGAs
- FMC (VITA 57) mezzanine site for I/O
- DDR2 SDRAM and QDRII SRAM memory resources
- Four x4 high-speed serial interconnects to the backplane or PCIe, Aurora or SRIO
- Additional low-speed I/Os to the backplane
- FusionXF Development Kit for HDL development
- 3U VPX with .8" pitch
- Air and conduction-cooled options

Benefits

- Dense FPGA resource in small 3U form factor
- Maximum I/O flexibility to front panel and backplane
- Excellent infrastructure for HDL development and host interaction
- Versatility for deployed or commercial environments

Overview

The FPE320 is a 3U VPX FPGA processor board that incorporates the largest Xilinx® Virtex®-5 FPGAs available with a FPGA Mezzanine Card (FMC) site. Providing many resources in a small, rugged form factor, the FPE320 is the ideal FPGA platform for 3U systems that need to acquire analog and other high-speed I/O, or that need a large FPGA processor.

Figure 1: FPE320 Architecture

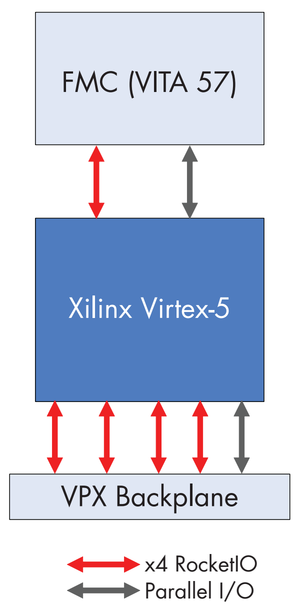


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Table 1: FPE320 FPGA Resource Table

	Logic Resources			Memory Resources			Clock Resources		Embedded Hard IP Resources & Speed Grades*				
	Slices	Logic Cells	CLB Flip-Flops	Max. Dist. RAM (kbits)	Block RAM/FIFO w/ ECC (36 kbits each)	Total Block RAM (kbits)	Digital Clock Mgrs. (DCMs)	Phase Locked Loop (PLL)/ PMCD	DSP48E Slices	PCIe Endpoint Blocks	PowerPC 440 Blocks	Speed Grade	RocketIO GTP (run at 3.125 GHz or lower)
LX330T	51,840	331,776	207,360	3,420	324	11,664	12	6	192	1	0	-1	20
SX240T	37,440	239,616	149,760	4,200	516	18,576	12	6	1,056	1	0	-1	20

* Note: These features are specific to using the FPGAs on the FPE320 and do not reflect all of the capabilities of the FPGAs themselves.

FPGAs have been become popular due to their impressive processing power, as well as their ability to meet size, weight, and power (SWaP) limitations. The inherent parallelism of FPGAs makes them well suited for a variety of image and signal processing applications, which have historically been addressed with a large array of general purpose processors. When complex algorithms are partitioned into FPGAs, users can see increases in performance that can lead to a dramatic reduction in slot count and system cost, both important factors in 3U systems.

As system platforms have grown smaller, many designers have considered 3U boards. 3U VPX has become an ideal platform for high-speed serial interconnects (HSSI) such as PCI Express® (PCIe), Aurora™, and Serial RapidIO® (SRIO) to the backplane, but board constraints have limited the use of large FPGAs with I/O. With the advent of the FMC site (see FMC overview, page 5), large FPGAs can be used in 3U systems because the I/O space requirements are minimized. FMC is a standard conceived to allow designers to take advantage of advances in the latest I/O (ADCs, DACs, etc.), coupling it directly to FPGAs. This allows users to take advantage of low latency and high-bandwidth that FPGAs support, while the flexibility of FMC eases design for multiple I/O and allows for dissipating heat more effectively. The FPE320 combines the I/O resources of the FMC with the backplane connectivity of 3U VPX to maximize the effectiveness of these many FPGA resources. The FPE320 is supported by the FusionXF Development Kit, which provides infrastructure and support for HDL development, software, and multi-processing applications, including PCIe, Aurora™ and SRIO. The processors that interact with the FPE320 support the Wind River® VxWorks® and Wind River® GPP Linux® operating systems.

Xilinx Virtex-5 FPGA

At the heart of the FPE320's processing is a Xilinx Virtex-5 FF1738 package FPGA, the largest FPGA in the Virtex-5 family. FPGAs provide parallel processing capabilities that can be used to reduce processor count and system size. Operations such as FFTs, FIR filters and other fixed-point and/or repetitive processing tasks are highly suited for placement inside FPGAs. A large FPGA node allows processing tasks to tackle input from the FMC mezzanine site or backplane I/O, or can simply function as an adjunct compute resource to the general purpose system processor.

The FPE320 supports Xilinx Virtex-5 LXT, SXT devices. Using the LXT for logic-intensive developers can tailor their hardware resources to match their algorithm needs (see the FPE320 FPGA resource table).

Curtiss-Wright Controls Embedded Computing supports the LX330T devices in the LXT family. With over 330,000 logic cells, the LXT family gives FPGA designers the most amount of space to program their algorithm. Within the SXT family, the SX240T device is supported. With 1,056 DSP slices and over 240,000 logic cells, the SXT device is ideal for A/D projects where the DSP48E slices can be used to maximum benefit.

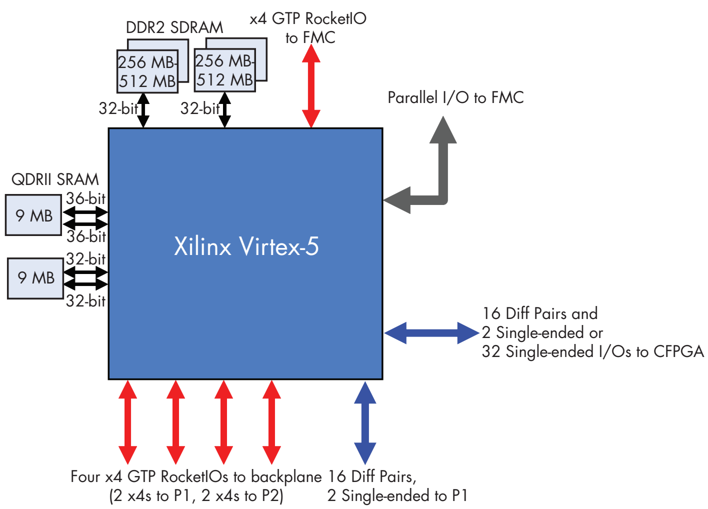
Larger Chips Reducing Development Time

The use of large FPGA nodes simplifies algorithm development, as processing can be done inside a single device or a reduced number of devices. When compared with the smaller package FPGAs, the larger FPGAs have more logic slices available. The availability of more logic gives designers greater freedom, making timing easier to close, and hence shortening development cycles. Additionally, as more FPGAs are used, greater complexity is needed to partition the algorithm and link the devices together. These I/O resources come at a greater expense in smaller devices, which already have less logic. When combined with a large amount of memory and I/O resources, the larger devices can fulfill processing needs for a variety of applications while still easing customer development.

FPGA Architecture

The FPGA nodes on the FPE320 have industry-leading I/O and memory resources to maximize the effectiveness of the devices in a variety of applications.

Figure 2: FPGA Memory and I/O Architecture



Memory

The memory resources on each FPGA node of the FPE320 give users the ability to process and store data sets for the most demanding applications.

Each FPGA node has both DDR2 and QDRII SRAM available. The DDR2 is organized into two banks, with each bank providing a x32 bus width using two x16 devices. Up to 512 MB of memory is available from each DDR2 bank, providing a large amount of storage space for data sets. Complementing the DDR2 are two independent banks of QDRII SRAM, for more processing-intensive tasks. The banks each have a x36 bus width, and provide immense bandwidth as they have separate read and write ports. Each bank is 9 MB, for a total of 18 MB available from each FPGA.
There is 128 MB of flash available for storing bit-streams, although they can also be loaded through the Configuration FPGA (CFPGA).

User FPGA I/O

The FPGA node on the FPE320 has an enormous number of I/O resources for connecting to other parts of the system. The FPGA compute node utilizes up to 20 RocketIO™ high-speed serial links, depending on which package is used. For the larger devices, such as LX330T and SX240T, 20 links are used. These links are divided between I/O to FMC and to the backplane. Parallel I/O is also used, with up to 148 lines routed to the dedicated FMC site, and 32 single-ended I/Os or 16 differential pairs and two single-ended I/Os routed to the CFPGA.

Table 2: GTP Speed/Clock Sources

Speed	Protocol	Clock Source
3.125 Gbps	Aurora, SRIO type 3	156.25 MHz
2.5 Gbps	Aurora, Serial FPDP, PCIe, SRIO type 2	125 MHz
2.125 Gbps	Aurora, Serial FPDP, 2x Fibre Channel	106.25 MHz
1.25 Gbps	Aurora, 1x Gigabit Ethernet	125 MHz
1.0625 Gbps	Aurora, Serial FPDP, 1x Fibre Channel	106.25 MHz

Cabling

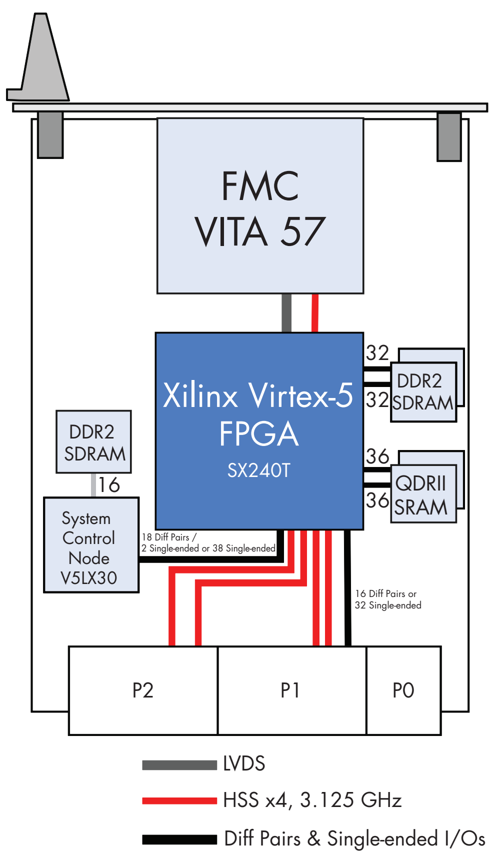
A JTAG cable is included with the board for programming of the FPGA.

Configuration FPGA & Chassis Management

The on-board CFPGA controls chassis management, temperature monitoring, JTAG, bit stream encryption, and routing of single-ended I/Os. The CFPGA has 128 MB of local DDR2 available for quick loading of bit streams using a 16-bit bus, and also has 4 MB of flash available for storing FPGA images. The CFPGA's ability to function as a switch for single-ended I/Os can be seen in the CFPGA I/Os diagram.

The CFPGA manages the images for itself and also for the FPGA processor. Images can be uploaded and stored in flash or SDRAM. SDRAM has the added advantages of speed and not retaining data when powered off. The volatile aspect of SDRAM is useful for some secure applications where no trace can remain when the board is not in use.

Figure 3: Differential Pairs and Single-ended I/Os



FMC (VITA 57)

PCI-X and other traditional open standard structures for I/O operations are less suitable for FPGA I/O, because they can slow data transfer rates while consuming valuable FPGA resources. FPGA I/O is inherently configurable and can be adapted to a wide range of I/O structures. FPGA I/O is best optimized when FPGAs are not treated the same way as CPUs, but connected directly with I/O devices or ports. The VITA 57 FMC open standard has been developed to capitalize on these FPGA attributes.

The FMC standard provides an industry standard mezzanine form factor in support of a flexible, modular I/O interface to an FPGA located on a baseboard or carrier card. It allows the physical I/O interface to be physically separated from the FPGA design while maintaining a close coupling between a physical I/O interface and an FPGA through a single connector, P1.

There is a choice of two very high-bandwidth connectors to interface the FMC to an FPGA on a carrier: a Low Pin Count (LPC) connector with 160 pins and a High Pin Count (HPC) connector with 400 pins. An FMC with the LPC connector can mate with a carrier that utilizes either an LPC or HPC connector.

The use of the FMC standard simplifies FPGA designs, reduces cost, and makes the design of I/O mezzanine modules simple and straightforward. Development cycles can be shortened and costs lowered by utilizing a single FPGA design in multiple applications, by simply mounting different FMC modules.

Typical FMC modules will have an I/O device, such as an ADC (with front end signal conditioning), buffer and connectors. Since FPGAs can interface directly to I/O devices' I/O pins, there is no need for bus interfaces (e.g., PCI) eliminating the need for bus converters and their associated overhead.

FMCs can be used to provide analog I/O, digital I/O, fiber-optic interfaces, camera interfaces, frame grabbers, additional memory or even dedicated DSP functions.

FMC modules are of a similar width, but half the size of PMC or XMC modules, and provide higher density host I/O.

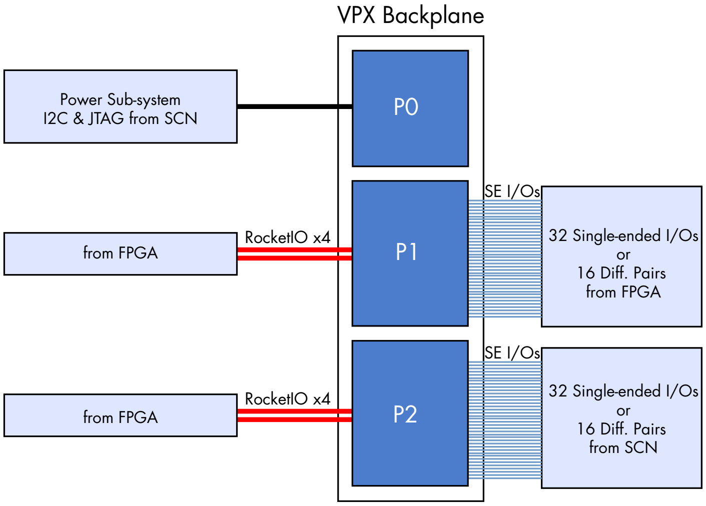
Key FMC features include:

- Up to 148 differential I/O pairs
- Up to 4 high-speed serial I/O links
- Air and conduction-cooled variants
- Module size 69 x 76.5mm

Backplane I/O

The backplane connectivity is shown below:

Figure 4: Backplane I/O Connectivity



Mezzanine Site

The FPE320 includes a versatile set of I/O options through a FPGA Mezzanine Card (FMC) site (VITA 57). FMCs provide flexibility for the latest I/O such as A/D converters, Serial FPDP (sFPDP) and LVDS, FMCs can also be designed by customers, following the VITA 57 standard.

FMC Site

The VITA 57 FMC site utilizes 148 user I/O pins from the dedicated FPGA nodes. Customer-developed, third party, or Curtiss-Wright FMC modules can be used with the FPE320. Announced FMC products from Curtiss-Wright include analog I/O boards which can be used to tailor the I/O capabilities of the FPE320 to customer project-specific needs.

Software and HDL

FusionXF FPGA Development Kit

The FPE320 uses the Curtiss-Wright FusionXF FPGA Development Kit to speed HDL development and to communicate with processors and other FPGAs in a system. FusionXF provides FPGA Hardware Development Logic (HDL) functions, application APIs, drivers, and utilities to simplify the task of integrating FPGAs into an embedded real-time DSP system design. It aids customers in the development of their FPGA algorithms and logic for Curtiss-Wright customer-programmable FPGA products, by providing all the building blocks to build a fully functional FPGA design into which a customer can integrate their FPGA logic and algorithms. FusionXF also provides mechanisms for communication between FPGAs as well as communication between FPGAs and processors. It includes example designs that show how to implement common FPGA functions such as control registers, DMA engines and interrupts, and also how to control these functions and communicate with them from software.

FusionXF is comprised of a Software Development Kit (SDK) and a Hardware Development Kit (HDK). The FusionXF SDK contains software libraries, drivers, and utilities for use in Windows, Wind River VxWorks, and Wind River GPP Linux environments. It facilitates the initialization and control of FPGAs, as well as the communication and movement of data between FPGAs and application software. Software drivers and libraries are provided to allow processing nodes to utilize FPGAs as co-processors, DMA engines, and memory pools. Utilities are provided to perform useful functions, such as loading new images into the FPGA's flash memory.

The FusionXF HDK contains HDL functions that are common to most FPGA applications, such as DDR and QDR memory controllers, RocketIO interfaces, parallel I/O interfaces, and commonly used FPGA functions such as DMA engines and register sets. In addition, there are HDL functions provided to implement protocols such as PCIe. The hardware independent HDL code resides in the VM Library. The hardware dependent HDL code resides in the BSIP.

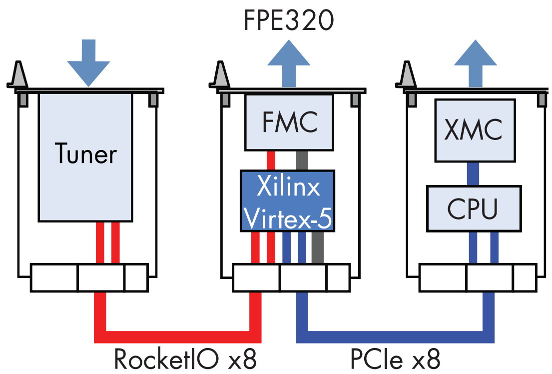
Flexible Architecture

The FPE320 has flexible architecture to support future products enhancements. The hardware supports a JTAG Player which could be implemented in the future with software upgrades. The FPE320 supports Open VPX profile 2F with the addition of support of Multi-Bus Sync Card (MBSC) and Bd_Reset and REFCLK_SE.

Example Applications

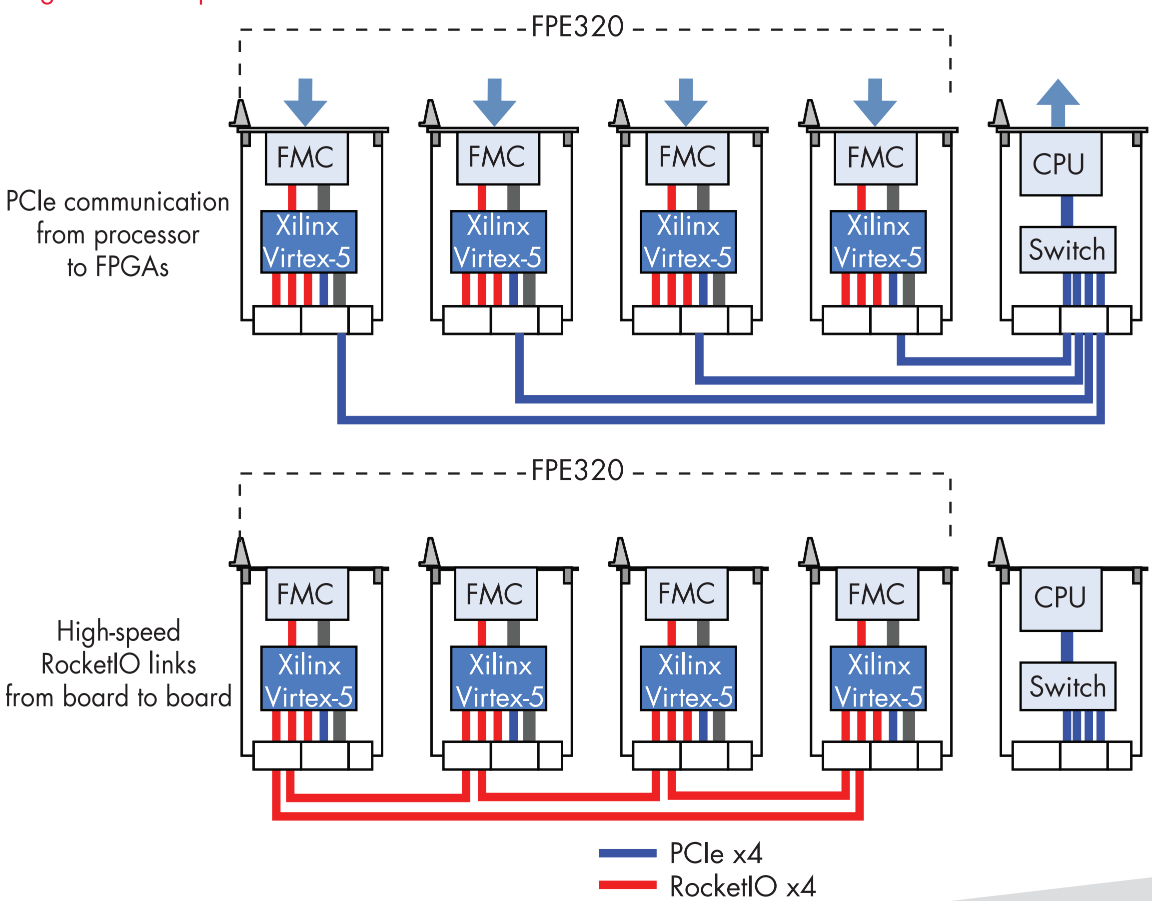
In Example 1, a three-slot system is shown with a tuner board, the FPE320, and a general purpose processor board with an XMC site. This small system provides a powerful signal processing engine that previously would have been done in a 6U system. The tuner processes data, and passes it along to the FPE320 using RocketIO, using the Aurora protocol. The FPE320 can then apply its large FPGA resources to the data, performing a variety of digital functions. The FMC is capable of outputting data for recording purposes, sending analog data to another source using a D/A FMC, or doing analog to digital conversion should the tuner output analog rather than digital data. The FPE320 is also acting as a bridge between the RocketIO coming from the tuner and the PCIe x8 interface to the processor board. The processor can then complete the processing, before outputting the data (using its XMC site) to storage or a display. All of this activity occurs in a 3-slot system, nicely tailored to applications with limited SWaP requirements.

Figure 5: Example 1



In Example 2, a 5-slot system is shown with four FPE320s and a processor board. Two interconnects are working in concert on the backplane. PCIe is used as the connection between the processor board and the FPE320s, allowing a data path to a general purpose processor, and providing the command and control infrastructure for the system. RocketIO is daisy-chaining the FPE320s together, providing a low-overhead, high-throughput infrastructure for the FPGAs to communicate with one another.

Figure 6: Example 2



The ADC510 is a standard FMC from Curtiss-Wright that provides two 12-bit, 500 MSPS channels of input to the FPE320. After this data is processed, it can travel to other FPE320s, or go directly to the processor using PCIe, before leaving the system. By leveraging the ability to add multiple FPE320s to a system, system designers can easily add additional channels and/or FPGA resources with a high-speed fabric, while still maintaining connectivity with a general purpose processor.



Table 3: Specifications

User FPGA	
Device	Xilinx Virtex-5 LX330T, SX240T
No. of FPGAs	1
Memory per FPGA	QDRII SRAM: 2x 9 Mbytes (36-bit data path) DDR2 SDRAM: 2x 256-512 Mbytes (32-bit data path) 128 Mbytes flash (storing of GFPGA images only)
Core FPGA	
Device	Xilinx Virtex-5 LX30
No. of FPGAs	1
Memory per FPGA	DDR2:128 Mbytes (16-bit data path) 4 Mbytes flash (storing of GFPGA images only)
Mezzanine	
Mezzanine Sites	1
VITA Specification	VITA 57
LX330T/ SX240T	Quad RocketIO 73 differential pairs 2 single-ended
Connectivity	
P0	Power, JTAG & SCN utility (I2C)
P1	2x 4 GTP RocketIO (PCIe to the backplane) 32 single-ended I/O or 16 differential pairs to Core FPGA
P2	2x 4 GTP RocketIO to backplane 32 singled-ended I/O or 16 differential pairs to User FPGA 8 dedicated single-ended I/O (7 to User FPGA and 1 to Core FPGA for Interrupt)
Software/HDL Code	
Operating System	Wind River VxWorks 6.5 (run on adjoining processor, not FPE320)
Utilities	Flash programming, diagnostics
HDL Code	FusionXF FPGA Development Kit, WindRiver Linux 3.0 after VxWorks 6.5

Standards	
Compliance	VITA 46.0, 46.4, 48, 57
Power/Mechanical	
Board Pitch	3U VPX 0.8”
Power VPX	Typ Pwr: 35 W Max Pwr: 55 W
Weight	AC: 1.05 lbs (470 g) CC: 1.21 lbs (547 g)
Cabling	JTAG cable and adapter (p/n JTAG-1002)



Table 4:
Environmental Specifications

		Commercial	Rugged	
			Air-cooled	Conduction-cooled
			Level 100	Level 200
Part Number Extension[1]		-	B1H	D5H
Temperature	Operational (at sea level)	0°C to +55°C (15 CFM air flow)[2]	-40°C to +70°C (20 CFM air flow)[2]	-40°C to +85°C (card edge temp)[3]
	Non-Operational	-40°C to +85°C	-50°C to +100°C	-55°C to +100°C
Vibration	Operational (Random)	-	0.04 g^2/Hz	0.1 g^2/Hz
Shock	Operational	-	20 g peak, 11 ms half sine	40 g peak, 11 ms half sine
Humidity	Operational	5-95% non-condensing	Up to 95%	Up to 95%
Altitude [4]	Operational	-	-15,000 to 60,000 ft	-15,000 to 60,000 ft
Conformal Coating [5]		No	Yes	Yes

Notes
1. Availability of the ruggedization levels are subject to qualifications for each product.
2. For operation at altitudes above sea level, the minimum volume flow rate shall be adjusted to provide the same mass flow rate as would be provided at sea level. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat. Some higher-powered products may require additional airflow.
3. The contacting surface on the rack/enclosure must be at a lower temperature to account for the thermal resistance between the plug-in unit and rack/enclosure.
4. Depending on the technology used, the risk for Single Event Upsets will increase with altitude.
5. Coated with Humiseal 1B31 or 1B73EPA. (ref. http://humiseal.com for details)

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

Technical Support

For technical support:

Website: www.cwcembedded.com/support

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