Fact Sheet

FMC-XCLK2

2GHz Multi-Channel Phase Matched Clock Generator

Applications

The FMC-XCLK2 is an ideal source for analog to digital converter sample clock for DSP applications including:

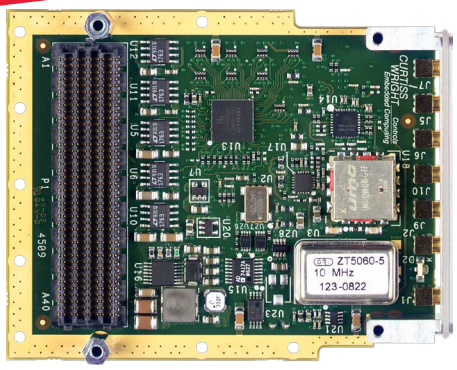
- Signal Intelligence (SIGINT)
- Spectral Analysis
- Radar

Features

- Four phase matched Radio Frequency (RF) outputs
- Selectable internal or external 10MHz reference (with frequency multipliers for RF output)
- External RF clock source
- FMC format
- Air-cooled and rugged build options

Benefits

- Provides a low cost, small form factor solution for low jitter clock sources
- Enables ease of synchronizing multiple acquisition cards
- Industry standard form factor



High-speed analog I/O solutions require good quality sample clock sources – often with multiple feeds to support an array of I/O converters. Such products are often expensive, bulky and not suited to embedded environment. The FMC-XCLK2 is different because it was designed with embedded computing in mind by providing a clock source, with up to four phase matched outputs, packaged in a convenient FMC board form factor for use with boards including Curtiss-Wright Controls Embedded Computing's FPGA based Digital Signal Processing (DSP) solutions.

The FMC-XCLK2 offers a number of clock source options used to generate the RF outputs. The most common source option is to use an on-board 10MHz temperature compensated crystal oscillator (TCXO) with low phase noise VCO/PLL fixed frequency multiplier circuitry to derive the desired RF outputs. The on-board 10MHz oscillator output can also be switched to the front panel to provide a reference to other system functions. The FMC-XCLK2 can alternatively use an external 10MHz source as master reference through a front panel connection. Output frequencies range from 50MHz to over 2GHz (each frequency output is a build variant) with a jitter of less than 0.5ps. Single-ended and differential clock outputs are supported.

When providing a clock source to multiple acquisition cards, users often need to synchronize the trigger, or start of acquisition for all cards, so that multiple samples are coherent. This is important for applications such as beam forming. The FMC-XCLK2 helps solve this problem by momentarily interrupting all sample clock outputs using its trigger/reset input when used with Curtiss-Wright Controls analog converter products. This gives time for all acquisition cards to be reset and to start to capture data synchronously.

The FMC-XCLK2 is an ideal clock source for Curtiss-Wright Controls' ADC512 (dual-channel 3GSPS 8-bit ADCs) and ADC511 (dual-channel 400MSPS 14-bit ADCs).

Learn More
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Table 1: Specification

RF Clock Outputs	
Output Frequency	Determined by a build option (when using 10MHz reference source)
Number of Channels	4 Single-ended or 2 Differential (build option)
Output Level	50 Ohm, AC coupled, LVPECL Output level at 800MHz typically 700mVp-p (single-ended)
Maximum Output Frequency	>2GHz
Connectors	Front Panel MMCX
Master/Slave 10MHz Reference Clock (to derive output frequency)	
On-board source	10MHz Temperature Controlled Crystal Oscillator (TCXO) Output to front panel (switch option) Output to FPGA host via FMC connector Output to RF multiplier
External source	Input from front panel (switch option) Output to FPGA host via FMC connector Output to RF multiplier
Front Panel Output Level	50 Ohm, AC coupled, TBA
Front Panel Input Level	50 Ohm, AC coupled, TBA
Front Panel Connector	MMCX (shared with 10MHz input and 10MHz output function)
External RF Clock Input	
Input Level	50 Ohm AC coupled -5 to +5 dBm recommended
Frequency Range	0 to >2GHz
Connector	Front panel MMCX1
Reset/Trigger	
Input Level	LVPECL (front panel) LVDS (FMC)
Front Panel Connector	MMCX
FMC	
Compliance	VITA 57.1
Power	
Supply	3V3_AUX, 3V3, 12V, 2.5V (VADJ)
Environmental	
Air-cooled Levels	L0 L100 (See Note)
Conduction-cooled Levels	L200 (See Note)
Leaded/RoHS Compliance	Build options

Note:
Designed to but not tested or verified

Table 2: Part Numbers

FMC-XCLK2-eefffffv	
ee	Environmental Build Level A0 Air-cooled Level 0 A1 Air-cooled Level 100 C2 Conduction-cooled Level 200
fffff	Frequency in MHz 0800 800MHz example 133M3133.3MHz example
v	Special Build Variant (includes all build options and special variants other than frequency, such as alternative connectors and leaded builds)

Note: New frequencies require a frequency tooling setup charge.

Figure 1: XCLK2 Block Diagram