Fact Sheet

CHAMP-FX3 (VPX6-472)

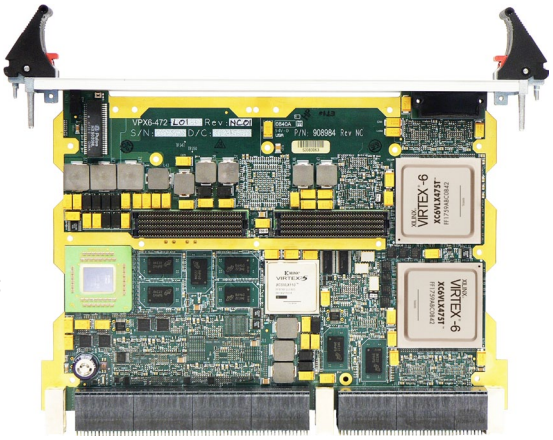
Xilinx® Virtex®-6 6U OpenVPX™ Module

Applications

- Radar Processing
- Signal Intelligence (SIGINT)
- ISR
- Image Processing
- Electronic Warfare

Benefits

- Dense FPGA resources combined with general purpose processing
- Maximum I/O flexibility
- Support of multi-processing applications
- Standards based – fits into emerging standard architectures



The CHAMP-FX3 is the next generation in Curtiss-Wright Controls Embedded Computing's family of user-programmable FPGA-based computing products, designed to meet the needs of challenging embedded high-performance digital signal and image processing applications. The CHAMP-FX3 combines the dense processing resources of two large Xilinx Virtex-6 FPGAs with a powerful AltiVec™-enabled dual-core Freescale™ Power Archtiecture™ MPC8640D processor, on a rugged 6U OpenVPX™-compatible (VITA 65) form factor module. The CHAMP-FX3 complements this processing capability with a rich assortment of rear-panel I/O and memories, including a Serial RapidIO® (sRIO)-based switching fabric, multiple high-speed serial links, and 20 pairs of LVDS links to the backplane that can be used to support Camera Link or other high-speed parallel interface. There are also two FMC sites that have been enhanced to support the next generation of FMC cards with 80 pairs of differential signals.

Using the CHAMP-FX3 along with Curtiss-Wright's Signal Acquisition FMC cards such as the ADC512/ADC513 provides a complete Digital Receiver Solution. Since FMCs have no FPGA on them and are lower power, they are better able to handle extreme rugged conditions. Furthermore with the flexibility of the FMC interface, alternate front ends can be accommodated by using different FMC modules.

This combination of enormous processing density and I/O flexibility make the CHAMP-FX3 an ideal choice for many commercial or rugged embedded applications including radar and signal intelligence, and for intelligence, surveillance and reconnaissance (ISR) platforms.

Learn More
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Features

- OpenVPX™ (VITA 65) profile MOD6-PAY-4FIQ2U2T-12.2.1-1, VPX REDI (VITA 48 option)
- Dual user-programmable Xilinx Virtex-6 FPGAs (SX475T or LX550T), each with:
  - 2 GB DDR3 SDRAM in two banks
    - Supports migration to 4 GB per FPGA
  - 72 MB QDRII+ SRAM in four banks
  - Four 5 GHz 4-lane serial links to the backplane
  - Three 5 GHz 4-lane serial links between the two FPGAs
  - One 4-lane sRIO 1.3 link to the onboard switch fabric
  - 20 LVDS pairs to the backplane
  - 20 differential pairs between both FPGAs
  - FMC connection with 80 differential signal pairs
- Freescale Power Architecture MPC8640D processor
  - Running at 1 GHz
  - 1 GB SDRAM in two banks
  - 256 MB flash
  - Two Gigabit Base-T Ethernet links to the backplane P4 connector
  - Two Gigabit Base-X Ethernet links to the backplane P4 connector
  - Two RS-232 links to the backplane
  - One x8 PCIe connection from the processor to the P5 backplane connector
- Two Mezzanine sites with support for FMC (VITA 57)
- Onboard sRIO 1.3 switch
  - Four 4-lane fabric ports to the backplane
  - 4-lane ports to both user FPGAs and the MPC8640D processor
- Thermal sensors for monitoring board temperatures
- Sensors for monitoring board power consumption
- Support for ChipScope™ Pro and JTAG processor debug interfaces
- Multi-board synchronous clock
- FusionXF BSP and FPGA design kit with highly-optimized IP Blocks, development environment, reference designs, scriptable simulation test benches and software libraries
  - VxWorks® and Linux® variants available
- Continuum IPC – inter-processor communications middleware available
- Continuum Vector subroutine library available
- VITA 48 1" pitch format
- Ruggedization levels
  - Level 0 (Commercial)
  - Air-cooled level 100
  - Conduction-cooled level 200

Figure 1: CHAMP-FX3 Block Diagram