Fact Sheet

CHAMP-FX2

Xilinx® Virtex®-5 based VITA 46/48 Module

The CHAMP-FX2 is a Freescale Power Architecture™ and FPGA-based VITA 46/48 computing platform targeted at demanding, high-performance signal and image processing applications such as radar, sonar, and signal intelligence. Providing a pair of state-of-the-art Xilinx Virtex-5 FPGAs for high-performance configurable logic, combined with an AltiVec™-enabled Freescale Power Architecture MPC8641 processor for general-purpose processing, command and control functions, and high-speed floating-point calculations, the CHAMP-FX2 gives developers enormous processing power in a package designed to meet both commercial and rugged environments.

The CHAMP-FX2 provides two user-programmable Virtex-5 FPGAs (LX110T or LX220T) combined with a dual-core MPC8641 processor. The heterogeneous design of the CHAMP-FX2 allows developers to optimize their designs by hosting the portions of their application on processing resources best suited to their application. The Virtex-5 LXT FPGAs give the user the largest gate count in the latest-generation FPGA architecture available, while the MPC8641D processor gives the user a high-performance general-purpose processor with an AltiVec-enabled floating-point vector engine.

The computing power of the CHAMP-FX2 is matched with ultra-high on-board and off-board I/O bandwidth. The new military aerospace COTS standard VITA 48 form factor allows the CHAMP-FX2 to offer a Serial RapidIO® (SRIO) switching fabric to connect the three computational nodes and the XMC mezzanine site with up to four x4 SRIO ports on the backplane connectors. Double Data Rate (DDR2) and Quad Data Rate (QDR-II+) complement the inter-node bandwidths by providing multiple, independent memory banks for each FPGA. Finally, high-speed serial ports connect the FPGAs to each other, the XMC site, and the outside world through either front-panel or back-panel connections. These connections, combined with a large set of discrete LVDS I/O signals, give the CHAMP-FX2 wide range of I/O options. The on-board MPC8641 gives the CHAMP-FX2 additional I/O in the form of dual Gigabit Ethernet, dual serial ports (EIA-232/422), and additional discrete I/O signals.

The CHAMP-FX2 offers a rich set of system and support software and tools designed specifically to ease the developer's task of integrating FPGA-based computation into a larger heterogeneous multicomputer application. Software and development tools for the CHAMP-FX2 are part of the Continuum Software Architecture (CSA). The Continuum FXtools package contains the full Continuum Firmware and BSP package, plus additional CHAMP-FX2 specific support libraries for the PowerPC using such off-the-shelf operating systems as VxWorks® and Linux™. The Continuum FXtools package also provides a set of highly optimized IP blocks (memory control, serial and LVDS interfaces, etc.), FPGA-specific function libraries (configuration, command bus mappings, etc.)and a scriptable FPGA simulation environment. The Continuum Vector algorithm library gives the MPC8641 a rich set of optimized signal and image processing functions utilizing the AltiVec unit. The Continuum IPC communications middleware package has been extended to directly support RapidIO-based transfers between the FPGAs and or between the FPGAs and other PowerPC-based nodes within the system. A SRIO endpoint block is also available.

The CHAMP-FX2 is designed to operate in rugged environments and is available in air- and conduction-cooled formats. Innovative cooling techniques are employed to handle high performance FPGA implementations. Rugged or commercial, the CHAMP-FX2 provides the developer with a flexible, high-performance computing platform in either a stand-alone or heterogeneous multi-computing environment. When combined with the various software packages, the developer can expect significant time-to-market/time-to-deployment improvements due to the high-performance IP blocks, tools, and communications infrastructure.

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Features

- Two user-programmable Xilinx Virtex-5 FPGA nodes (LX110T or LX220T) each with:
  - Two banks of DDR2 per FPGA node (512MB total). Up to 4.4GB/s peak bandwidth per FPGA
  - Four banks of QDR-II+ per FPGA node (36MB total). Up to 8.8GBB/s peak bandwidth per FPGA
  - 1.25GB/s serial connection between the nodes
  - Two high-speed 4-lane serial connections to the backplane
  - 18 pairs (36 pins) of discrete LVDS signals from each FPGA to the backplane
- One Dual-core MPC8641 processor
  - Running at 1GHz
  - Up to 1GB of DDR2 with ECC
  - 512MB of Flash with write protection for user code, data, or FPGA bitstreams
  - Protected backup Flash
  - 128KB NVRAM
  - Two Gigabit Ethernet interfaces
  - Two serial ports (one EIA-232 and one EIA-242/422)
  - Connections to the FPGA configuration bus and command/control bus
- On-board SRIO switch
  - Connection to the Freescale Power Architecture processor
  - One port to each FPGA node. Additional port to the XMC site
  - Four ports to the backplane
- XMC site
  - 8-lane PCI Express® connection to the Freescale Power Architecture processor. This may be user-configured to form a 4-lane SRIO connection to the fabric
  - High-speed serial connection to each FPGA node
- Thermal sensors for monitoring board temperatures
- Sensors for monitoring FPGA power consumption
- Support for ChipScope Pro and JTAG processor debug interfaces
- Multi-board synchronous clock
- Continuum FXtools FPGA design kit with highly-optimized IP Blocks, development environment, reference designs, scriptable simulation test benches and software libraries
- Continuum Firmware and BSP for VxWorks and Linux and systems library kit for the MPC8641 processor
- SRIO Endpoint Block available
- Continuum IPC – inter-processor communications middleware available
- Continuum Vector subroutine library available
- VITA 48 1" pitch format
- Range of air- and conduction-cooled ruggedization levels available

Figure 1: Hardware Architecture

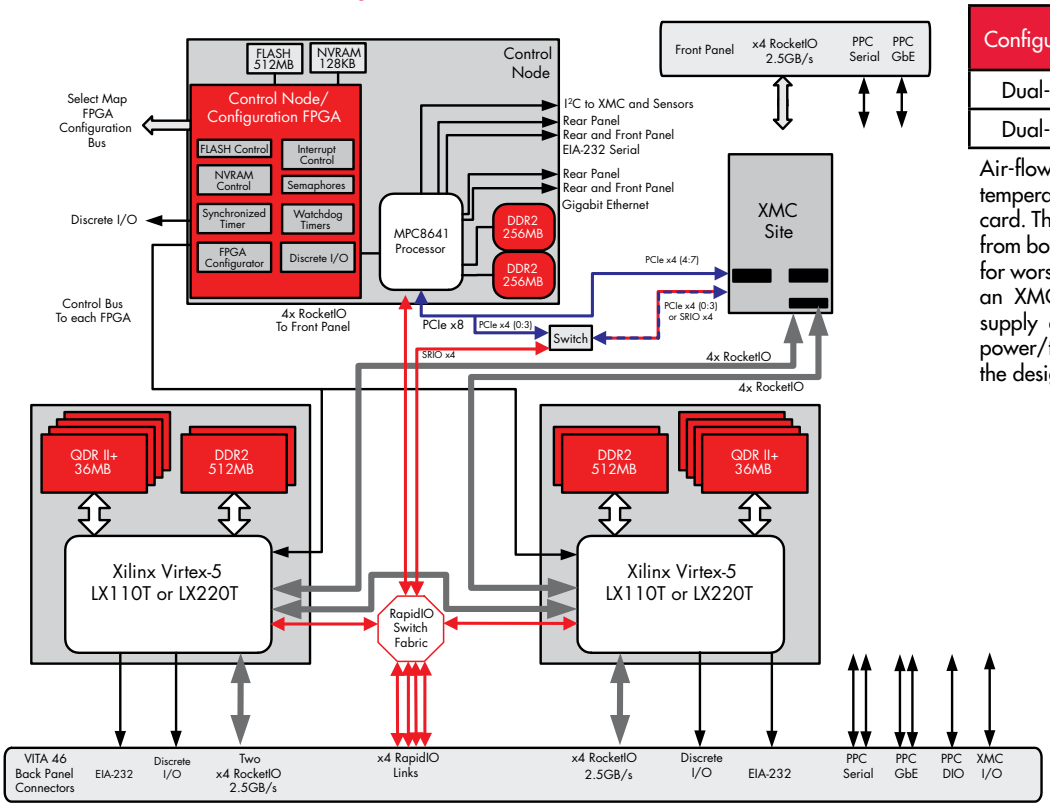

Table 1: Cooling Air Requirements

Configuration	Temperature Range	Air-flow
Dual-core	0° - 55°C	15 CFM
Dual-core	-40° - 71°C	24 CFM

Air-flow is specified for sea-level conditions. The temperature refers to the inlet temperature at the card. The CHAMP-FX2 requires cooling air to flow from bottom to top. The air-flow specifications are for worst case (highest power) conditions, without an XMC installed. Curtiss-Wright Controls can supply additional recommendations for specific power/temperature/altitude scenarios to support the design and testing of cooling subsystems.

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