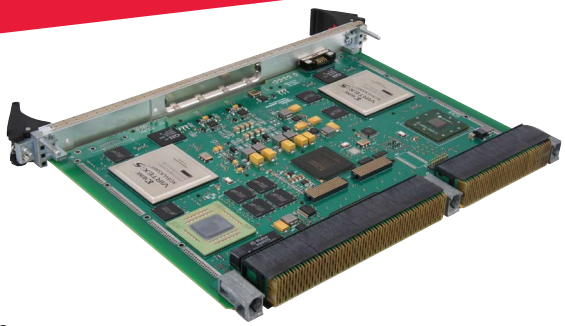
Data Sheet

CHAMP-FX2

FPGA Accelerator Signal Processing Platform



Features

- 6U VPX-REDI (VITA 46 and 48) FPGA signal processing platform
- Two user-programmable Xilinx® Virtex®-5 FPGA nodes (LX110T or LX220T) with:
  - Two banks of DDR2 per FPGA node (512MB per node, up to 1GB)
  - Four banks of QDR-II+ per FPGA node (36MB per node)
  - 1.25GB/s serial connection between the nodes
  - Two high-speed 4-lane serial connections to the backplane
  - 18 pairs (36 pins) of discrete LVDS signals from each FPGA to the backplane
- One dual-core Freescale Power Architecture™ MPC8641 processor
  - Running at 1GHz
  - 1GB of DDR2 with ECC
  - 512MB of Flash with write protection for user code, data, or FPGA bitstreams
  - Protected backup Flash
  - 128KB NVRAM
  - Two Gigabit Ethernet (GbE) interfaces
  - Two serial ports (EIA-232 or EIA-422)
  - 16 discrete I/O signals
  - Connections to the FPGA configuration bus and command/control bus
- On-board Serial RapidIO® (SRIO) switch
  - One 4-lane port to the PowerPC™ node
  - One 4-lane port to each FPGA node
  - Additional 4-lane port to the XMC site
  - Four 4-lane ports to the backplane
- XMC site
  - 8-lane PCI Express® (PCIe) connection to the PowerPC node, user-configurable to make a 4-lane SRIO connection to the on-board RapidIO switch
  - One 4-lane high-speed serial connection to each FPGA node
- Thermal sensors for monitoring board and processor temperatures
- Sensors for monitoring FPGA power consumption
- Support for ChipScope™ Pro and JTAG processor debug interfaces
- Continuum FXtools FPGA design kit with:
  - Continuum Middleware and BSP package for VxWorks® and Linux® and systems library kit for the MPC8641
  - Highly-optimized VHDL libraries
  - Reference designs
  - Scriptable System Verilog (IEEE 1800™) simulation test bench
  - Software libraries
  - SRIO IP block available
  - CamerLink IP block available
- Continuum IPC – inter-processor communications firmware available
- Continuum Vector subroutine library available
- Commercial variants, as well as a range of air- and conduction-cooled ruggedization levels available

continuum FXTOOLS

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Overview

The CHAMP-FX2 is a reconfigurable computing platform designed to tackle demanding DSP tasks such as image processing, radar, data compression, and signal intelligence. Utilizing the massive parallelism and rapid reconfigurability of FPGAs, combined with the flexibility of an AltiVec™-enabled dual-core PowerPC processor, the CHAMP-FX2 platform is well suited to replace either dedicated ASIC-based hardware or large arrays of processors for front-end signal or image processing, where sustained data rates and processing performance are important to overall system performance, or general algorithm acceleration tasks where data is pushed into the FPGA for calculation performance that may take 10's of general purpose processors to achieve. Many algorithms such as FFTs, 1D and 2D convolutions and filters on incoming data streams may be efficiently implemented in FPGAs. FPGA technology allows unequaled parallelism and enables pipeline processing, typical in DSP applications. Benefits include overall slot reduction, increased processing density and system cost reduction.

The CHAMP-FX2 provides a balanced mix of mezzanine interfaces, high bandwidth I/O, a variety of high-performance FPGA memories, off-board fabric connectivity with FPGA and general-purpose processing resources. The 6U VPX-REDI board features two Xilinx Virtex-5 LXT platform FPGAs (LX110T or LX220T) for user-defined functionality, as well as a dual-core MPC8641D processor, all connected by a high-speed SRIO switching fabric. The board architecture provides a flexible standalone or system-level platform for solving a variety of signal processing challenges. Variants of the CHAMP-FX2 are designed to operate in either commercial or rugged environments and are available in air- and conduction-cooled formats.

Thermal and power management is a critical factor when designing with large FPGAs. The CHAMP-FX2 provides the ability to monitor the FPGA die and board temperatures as well as the amount of current consumption of each FPGA through the user interface. The CHAMP-FX2 supports a flexible FPGA configuration manager. This allows the designer to store multiple FPGA configuration files in Flash or DDR2 memory. The ability to store configuration files in volatile memory is useful for fast FPGA reconfiguration and storage of classified data or algorithms. Each FPGA may be easily reconfigured with alternate configuration files via commands from either the on-board PowerPC node or any Curtiss-Wright Controls PowerPC node on the RapidIO fabric.

The Continuum FXtools design kit provides a rich set of PowerPC and FPGA-based functions enabling rapid prototyping and deployment of FPGA-based systems. In addition to the full Continuum Firmware and BSP package for the PowerPC, FXtools contains a library of highly-optimized VHDL IP blocks including dual-port memory controllers, PCIe core wrapper, scalable switching interconnect, and advanced DMA engines. Based on the Xilinx ISE™/EDK design flows these blocks can be combined with other off-the-shelf or custom IP blocks to rapidly implement complex, system-on-chip designs. To support this, FXtools includes a set of design templates and example designs, as well as a SystemVerilog (IEEE 1800) simulation testbench with a full set of bus functional models and scripting capabilities. The CHAMP-FX2 provides a JTAG header to support the use of Xilinx ChipScope™ Pro and JTAG development tools. Refer to the Continuum FXtools datasheet for more details.

To integrate the two user FPGAs into a larger SRIO network, a SRIO Endpoint block is also available. Sold separately, this high-performance endpoint can act either as a target or initiator (supporting NWRITE, NWRITE_R, SWRITE, and NREAD operations) for either memory-mapped or streaming transfers (target or initiator) with a similar advanced DMA engines as found in other FXtools IP blocks.

Operational Modes

Depending on system processing requirements, the CHAMP-FX2 may be used alone or in conjunction with other system elements. The CHAMP-FX2 supports the following modes of operation:

- Standalone: Does not require other boards in the system for initialization, configuration, development or deployment. The on-board PowerPC node executes code from Flash memory and performs all board-level control and status functions.
- System implementation: The board is combined with other VPX boards such as the CHAMP-AV6 or VPX-185 Single-Board Computer (SBC). The on-board PowerPC becomes a peer-computing resource to these other processor-based boards and the FPGAs become computing resources accessible from any node within the system.

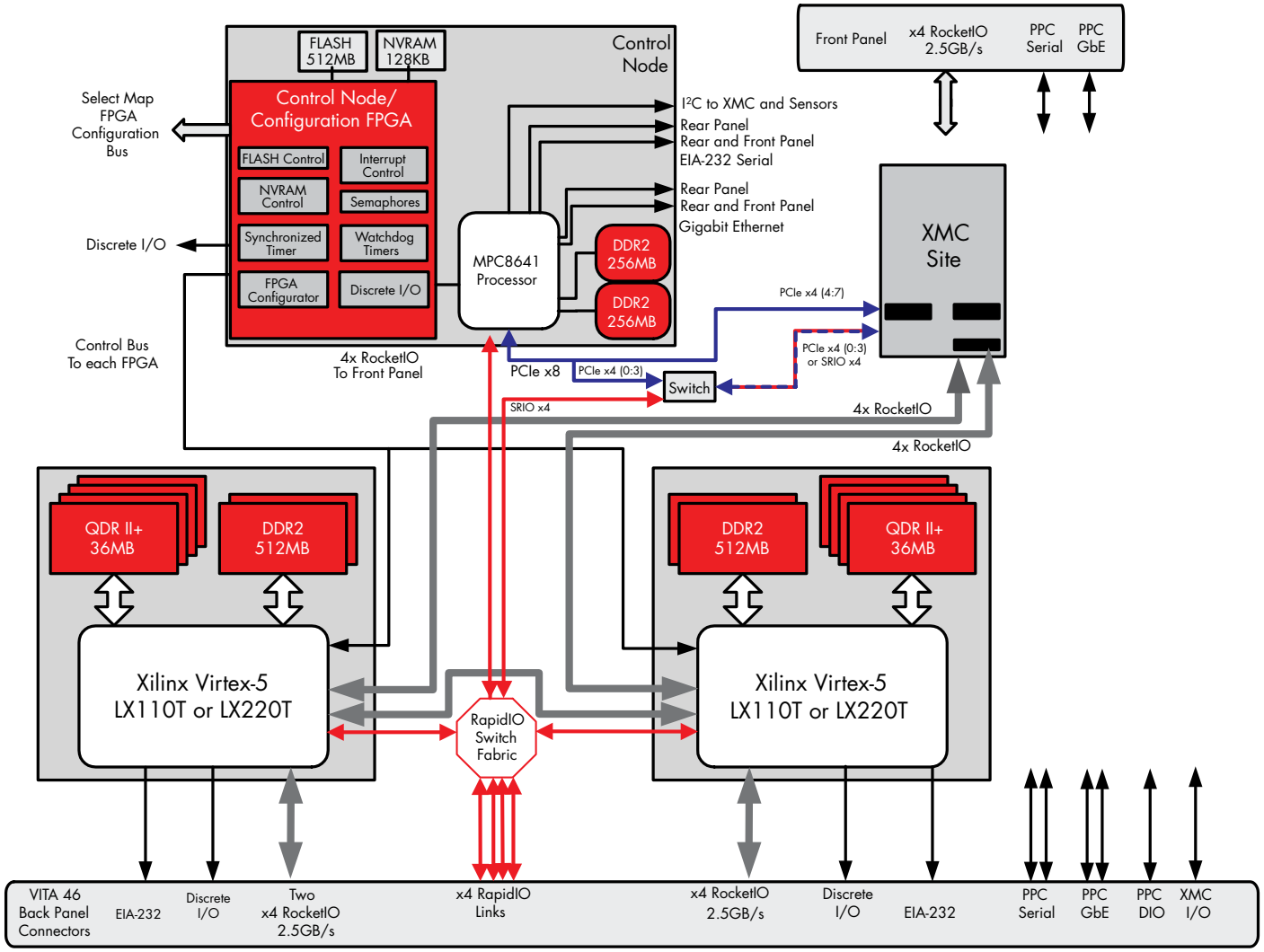


Architecture

The CHAMP-FX2 architecture (seen in Figure 1) is suited to DSP applications that place a high premium on sustained I/O throughput, FPGA memory bandwidth and off-board fabric connectivity through either the XMC mezzanine port, back-panel serial ports, or the RapidIO fabric. The data flow capabilities of the CHAMP-FX2 ensure that applications can extract the most from the raw computing performance of the two Virtex-5 platform FPGAs. The CHAMP-FX2 architecture encompasses a number of key attributes that contribute to maximizing DSP performance:

- Two Virtex-5 LXT platform FPGAs and a dual-core MPC8641D processor
- High-speed SRIO switching fabric connecting the FPGAs, the PowerPC node, and the rest of the multicomputer – up to 2.5GB/s bidirectional per port
- High-speed serial connectivity (RocketIO™) between the FPGAs, to the backplane, and to the XMC Mezzanine site – up to 20GB/s total off-board serial bandwidth
- 13.2GB/s peak memory bandwidth per FPGA using two DDR2 banks and four QDR II+ banks
- Out-of-band control bus for FPGA application command and control

Figure 1: CHAMP-FX2 Architecture



Virtex-5 LXT Details

The Virtex-5 LXT devices used on the CHAMP-FX2 are the largest gate count components in the Virtex-5 family. Each device contains a high density array of logic cells, XtreamDSP48E™ slices and multiple on-chip memory banks that enable high-speed vector processing. These FPGAs allow Gigabit-level connectivity for high-bandwidth, low-latency FPGA communication. Table 1 highlights the Virtex-5 LXT capabilities found on the CHAMP-FX2.

The Virtex-5 LXT offers a number of features that are either enhancements over earlier generation Virtex components or are entirely new to the Virtex-5. The 65nm ExpressFabric™ logic gate technology of the Virtex-5 is the first to use a 6-input LUT which enables more logic to be packed into a single logic cell and thereby increase speed and area utilization. The Distributed RAM is a 256-bit memory per CLB with 64-bits per LUT, while the Block RAM has been increased to 36-Kbit dual-port blocks with independent clocking on each port. The BRAM memories can be easily configured as single-port, dual-port, or FIFO memory structures and are instrumental in achieving high performance in DSP applications. The DSP48E slices have been enhanced with a 25 x 18 multiplier and a 48-bit adder to enable single-precision floating point math and wide filters with fewer slices. These features are combined with various power-saving features to make the Virtex-5 LXT an ideal choice for high-performance embedded computing.

Table 1: Virtex-5 LXT capabilities found in the CHAMP-FX2

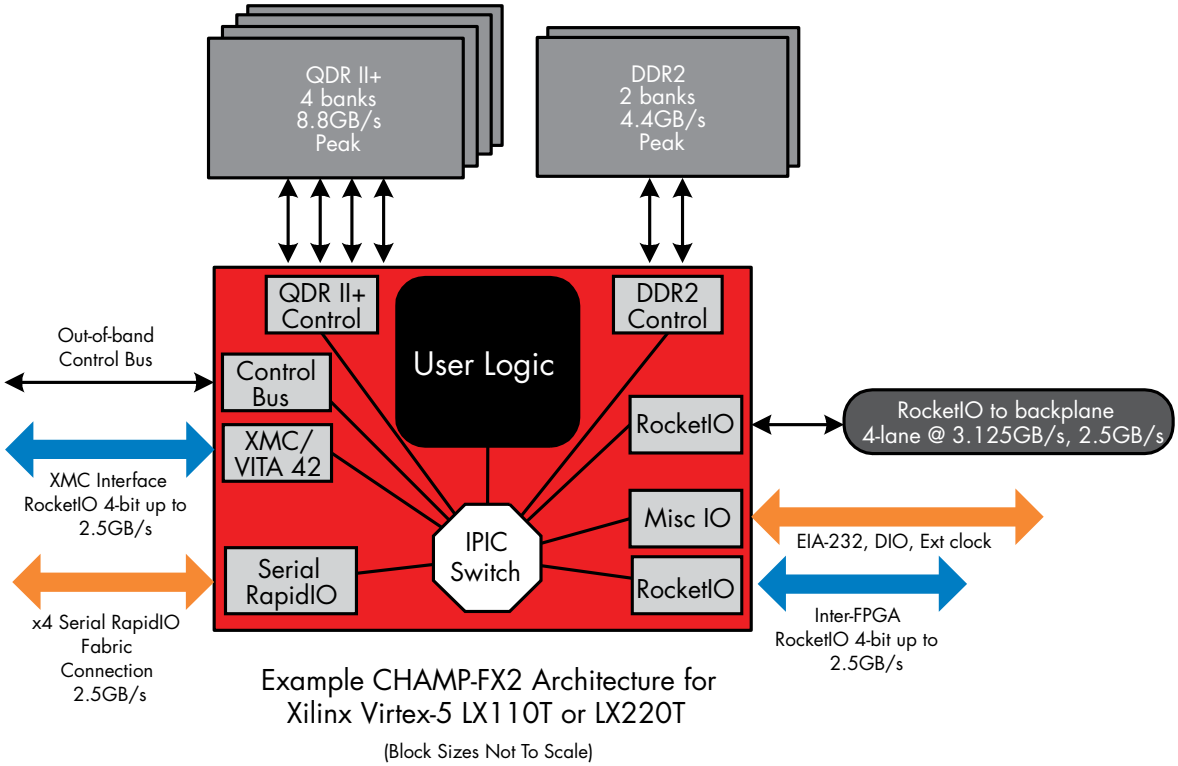
	CLB Resources				Memory Resources			Clock Resources		Embedded Hard IP Resources	
	CLB Array Size (Row x Column)	Slices	Logic Cells	CLB Flip-Flops	Max Dist. RAM (kbits)	Block RAM/ FIFO w/ECC (36-kbits each)	Total BRAM (kbits)	Digital Clock Manager (DCM)	Phase Locked Loop (PLL)/ PMCD	DSP48E™ slices	PCI Express Endpoint Blocks
LX110T	160x54	17,280	110,592	69,120	1,120	148	5,328	12	6	64	1
LX220T	160x108	34,560	221,184	138,240	2,280	212	7,632	12	6	128	1

User FPGA Architecture

Each user FPGA has a variety of external I/O and memory interfaces as shown in Figure 2. Some or all of the following interfaces may be implemented in a user FPGA design:

- Up to four independent QDR II+ interfaces
- Up to two independent DDR2 interfaces
- Up to four off-chip, 4-lane RocketIO interfaces using Aurora™ protocol
- SRIO Endpoint
- Control bus interface
- Switching interconnect

Figure 2: External I/O and Memory Interfaces



Example CHAMP-FX2 Architecture for Xilinx Virtex-5 LX110T or LX220T

(Block Sizes Not To Scale)



DDR2

Each FPGA node interfaces to two, 256MB or 512MB, 32-bit banks of DDR2 for a total of 512M or 1GB. The instantaneous peak data transfer rate to the pair of banks is 4.4GB/s. The DDR2 interface may be implemented as two independent 2-bit interfaces or a single 64-bit interface. The DDR2 is intended for temporary data storage, historical data storage and as a scroll buffer. The DDR2 controller IP block is structured as a dual port interface to facilitate pipeline designs that have dedicated read and write port structure.

QDRII+

Each FPGA node interfaces to four 9MB, 36-bit banks of QDR II+ for a total of 36MB. The instantaneous peak data transfer rate 8.8GB/s. The QDR-II+ interface may be implemented as four independent 36-bit interfaces, two 72-bit interfaces or a single 144-bit interface. The QDR-II+ is intended for temporary data storage associated with DSP algorithms like FFTs or filters. The QDR-II+ controller IP block is structured as a dual port interface to facilitate pipeline designs that have dedicated read and write port structure.

Serial RapidIO Switched Fabric

The CHAMP-FX2 utilizes SRIO interconnect to provide high-speed processor to processor communications. Using the native SRIO port of the MPC8641 as well as RocketIO GTP transceivers with the optional SRIO Endpoint block on the two FPGAs, the processor and both FPGAs each have a 4-lane interface capable of simultaneous 1.25GB/s transmit and receive for a total of 2.5GB/s of communications bandwidth per port. A Tundra TSI578 SRIO switch provides local switching as well as routing the three processor SRIO ports and the single XMC SRIO port to the VPX core fabric connectors. Multiple VPX cards like the CHAMP-FX2, CHAMP-AV6, or VPX-185 SBC may be inter-connected using the SRIO core fabric interface. The four SRIO ports support a maximum bandwidth of 5GB/s transmit and receive for a total of 10GB/s. The on-board switch function facilitates building systems of multiple cards without an external switch card.

Serial RocketIO Connectivity

Xilinx RocketIO GTP transceivers are used extensively on the CHAMP-FX2. In addition to the connections to the SRIO switching fabric, 4-lane RocketIO ports are used to connect the two FPGA nodes together, connect each FPGA node to the mezzanine site, and to provide a connection from each FPGA directly to the backplane. These connections allow for a variety of serial interconnect technologies to be used for on- and off-board connectivity such as Xilinx Aurora™, PCIe or SRIO. Configured as bi-directional, 4-lane links, these paths provide low latency, high performance FPGA or sensor interconnects. All links may operate up to 3.125GB/s. (bi-directional bandwidth 2.5GB/s). These links can also be controlled using a SW programmable clock device.

XMC (VITA 42)

The CHAMP-FX2 is equipped with one XMC (VITA 42) mezzanine site. The primary interface is switched to allow either an 8-lane PCIe (VITA 42.3) connection from the MPC8641 processor capable of 2GB/s of bidirectional bandwidth or a 4-lane SRIO (VITA 42.2) connection to the switch fabric providing up to 2.5GB/s bidirectional bandwidth. Additional connectivity to each of the FPGA nodes on the CHAMP-FX2 is provided by a pair of 4-lane RocketIO connections 2.5GB/s bidirectional bandwidth each.

The conduction-cooled versions of the CHAMP-FX2 adhere to the IEEE 1386-2001and ANSI/VITA 20 standard for conduction-cooled PMCs. The CHAMP-FX2 thermal frame provides the best possible thermal interface for mezzanine modules by supporting the primary and secondary thermal interfaces as defined by ANSI/VITA 20. To support high power XMC modules, the CHAMP-FX2 thermal frame supports a mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed XMC modules can significantly lower the temperature rise between the CHAMP-FX2 card edge and the XMC components. The mid-plane thermal shunt does not impinge on the IEEE 1386-2001 specified component height.



SelectMAP & Command Bus

The CHAMP-FX2 includes two additional communication paths that are not found on Curtiss-Wright Controls' PowerPC-based VPX products. The SelectMAP interface is a set of connections from the PowerPC node utility FPGA to each of the user FPGAs and is used for configuring the user FPGAs. The command bus is an additional out-of-band communications bus that connects the PowerPC to the two user FPGA nodes. The command bus is used primarily to give command and control instructions to the application running on the two user FPGAs without interfering with data movements in or out of the primary SRIO interfaces.

LVDS Discrete Digital I/O

Each user FPGA provides thirty-six general purpose LVCMOS25/LVDS25 I/O lines (or 18 LVDS pairs) which are accessible at the backplane connector. Three of these pairs may be used as differential clocks. Each bit is individually programmable to be an input, output or I/O. All bits configured as an input may be used to trigger an interrupt which is further programmable to be level or edge sensitive. Both levels and transition directions may be detected.

Control Node Architecture

The control node on the CHAMP-FX2 is an AltiVec-enabled dual-core MPC8641D processor running at 1GHz. The MPC8641D provides in a single package two e600 cores, dual DDR2 memory controllers with ECC, a SRIO interface, a PCIe interface, GbE controllers and serial I/O controllers. The e600 core and AltiVec units of the MPC8641D processor are based on the proven internals of the MPC7448 processor, offering a large 1MB internal L2 cache. Existing C, assembly and AltiVec assembly code will run on the MPC8641D without change.

Double Data Rate DDR2

Control node on the CHAMP-FX2 supports 1GB of DDR2 using the dual memory controller feature of the MPC8641 processor, providing a peak memory bandwidth of 6.4GB/s. The memory is protected with Error Checking and Correcting (ECC) circuitry that can detect and correct all single-bit errors and detect all double-bit errors. The high memory bandwidth will support demanding streaming data applications with simultaneous occurrence of dataflow from the processors and SRIO interfaces.

Flash Memory

The CHAMP-FX2 is equipped with 512MB of Flash memory. The 32-bit wide interface supports peak transfer rates of 100MB/s to minimize boot and program loading times. For absolute security against inadvertent Flash programming or corruption, a hardware jumper is provided to disable write access to the Flash.

Permanent Alternate Boot Site (PABS)

The CHAMP-FX2 has a secondary Flash subsystem, PABS, which provides a backup boot facility. PABS is typically used in two scenarios. The first is recovery from corruption of the primary Flash memory. The CHAMP-FX2 can be made to boot from PABS by asserting a control signal on the backplane or via an on-board jumper. Once the PABS resident firmware is booted the main Flash can be programmed to re-instate the standard firmware. The second scenario is the support of de-classification requirements. PABS firmware provides de-classification functions that will scrub the contents of main Flash. Since the PABS Flash is hardware write-protected, the user is ensured that no classified data can be written inadvertently to PABS.

Serial Ports

The CHAMP-FX2 provides one EIA-232/EIA-422 serial port and one EIA-232 port to the control node processor. Each EIA-232 serial port uses the MPC8641 DUART to support asynchronous communications with one transmit and one receive signal. Both ports are connected to both a front panel connector and the backplane connector. One serial port allows the use of the DTR signal to automatically detect the connection of a data terminal and can be used to control the boot-up sequence of the card if desired. The other port can be configured to be an EIA-422 differential serial port utilizing the MPC8641 DUART. The EIA-422 port supports asynchronous communications with one transmit and one receive pair. The EIA-422 port is connected to the backplane connector. The EIA-232 ports support operation up to 115200 baud, while the EIA-422 port supports a maximum of 20Mbaud.



LVTTL Discrete Digital I/O

The control node provides sixteen general purpose discrete I/O lines which are accessible at the backplane connector. Each bit is individually programmable to be an input, output or I/O. All bits configured as an input may be used to trigger an interrupt which is further programmable to be level or edge sensitive. Both levels and transition directions may be detected.

Utility Features Mailbox, Semaphores & Timers

The CHAMP-FX2 features a number of utility features to facilitate multi-processor software applications. Each processor core has a mailbox interrupt mechanism whereby a processor can interrupt another processor and deliver a 32-bit value. The board provides sixteen hardware semaphore registers which are typically used to coordinate the sharing of hardware resources between multiple tasks. The hardware solution provides a faster alternative to traditional software/memory techniques and avoids the use of shared memory to access the semaphores. In addition to the timer resources within the MPC8641D, the CHAMP-FX2 provides six general purpose 32-bit timers which may optionally cause an interrupt to any core upon rollover and be preset with an interval value.

Avionics Style Watchdog Timer

The CHAMP-FX2 provides a watchdog timer for each of the processor cores. Each watchdog timer is a pre-settable downcounter with a resolution of 1 µsec. Time-out periods from 1 second to 32 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, a backplane signal can be asserted to disable all watchdog interrupts. The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in "Avionics" mode whereby a minimum interval between writes to the watchdog register is also enforced. In other words, writing to the watchdog register too soon or too late causes an exception event.

Multi-board Synchronous Clock

The CHAMP-FX2 includes a special purpose counter which may be synchronized with corresponding counters on other boards in the same system. This common time base allows a developer to time-stamp messages and/or data buffers, with the knowledge that the local time is maintained at the same value by all the boards in the system. The counter can be set to roll-over to a pre-load value and interrupt on roll-over. This feature is typically most valuable for debugging and instrumenting multi-board applications code, which can present challenges in coordinating the distribution of data items between processors.

Thermal Management

The CHAMP-FX2 contains temperature sensors that monitor the board and processor temperature. Thermal management is key when dealing with large FPGAs that can consume a significant amount of power. Two sensors are located along each edge of the board, and one sensor per processor (the control node and both user FPGAs) is provided. The control node monitors the sensors through an I2C bus. The thermal sensors provide a programmable over-temperature status that is used to illuminate a red LED as well as provide an interrupt to the system. The software API allows the application to poll the board and die temperatures during development and deployment.

Power Management

The CHAMP-FX2 provides current monitoring circuitry to report each FPGA's power consumption. The software API enables the user to monitor the individual FPGA power consumption.

Indicator LEDs

The CHAMP-FX2 provides ten user controllable LEDs. Four of these are visible on the front panel of both air- and conduction-cooled versions. There is an additional red LED on the front panel of both versions used to indicate a failure determined by the on-board diagnostic firmware. The other six LEDs are located on card, but are not visible from the front.



Continuum FXtools

Continuum FXtools is the developers kit for the CHAMP-FX2 and includes the following functionality:

- The full Continuum Middleware and BSP package for the PowerPC (VxWorks, contact factory for Linux or other OS availability)
- CHAMP-FX2 Hardware, Software, and Firmware User's Manuals
- High-performance IP block library
- Example reference designs
- SystemVerilog (IEEE 1800) Modelsim® simulation testbench
- Support for Xilinx ISE, EDK, and ChipScope Pro tools
- Optional SRIO Endpoint Block also available
- Optional CamerLink Block also available

Refer to the Continuum Middleware and BSP and the Continuum FXtools datasheet for more details.

Options

Contact the factory for configurations options.

Specifications

The CHAMP-FX2 is available in a full range of environmental grades starting from commercial air-cooled to extended temperature, rugged, conduction-cooled versions. This allows the customer to select the board to match the environmental requirements of the platform. The tables below show the power, dimensions and weight of the board.

Table 2: FPGA Power

FPGA complement	Maximum Power			Typical Power		
	12V	5V	3.3V Aux	12V	5V	3.3V Aux
LX220T	99W	39W	0.1W	86W	34W	<0.1W
LX110T	94W	37W	0.1W	81W	32W	<0.1W

Note that the power consumption of the CHAMP-FX2 is highly dependent on the application loaded onto the FPGAs and the PowerPC processor. The above data is given as guidance only.

Table 3: Dimensions and Weight

Dimensions and Weight		
Option	Dimension	Weight
Air-cooled	Per VITA 48.1	904g
Conduction-cooled	Per VITA 48.2	1167g

Table 4: Cooling Requirements

Cooling Air Requirements	
Temperature Range	Air-flow
0° - 55°C	15 CFM
-40° - 71°C	24 CFM

Air-flow is specified for sea-level conditions. The temperature refers to the inlet temperature at the card. The CHAMP-FX2 requires cooling air to flow from bottom to top. The air-flow specifications are for worst case (highest power) conditions, without an XMC installed. Curtiss-Wright Controls can supply additional recommendations for specific power/temperature/altitude scenarios to support the design and testing of cooling subsystems.



Part Numbers

Check with a Curtiss-Wright Controls representative for availability of specific part numbers.

VPX6 - 470 - UVWXYYY

- Y denotes a specific configuration that typically describes: clock configurations, memory and other configurable options.
- X denotes the processor configurations: (size of FPGAs and PowerPC speeds)
- W denotes the mechanical format:
  - 4: 1" pitch
  - 5: 1" pitch, 2-level maintenance support
- V denotes the temperature range:
  - 0: 0°C to 50°C
  - 1: -40°C to 71°C
  - 2: -40°C to 85°C
- U denotes the cooling method:
  - A: air-cooling
  - C: conduction-cooling

A formal quote from Curtiss-Wright Controls or authorized representative will provide a complete part number and description of the configuration.

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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