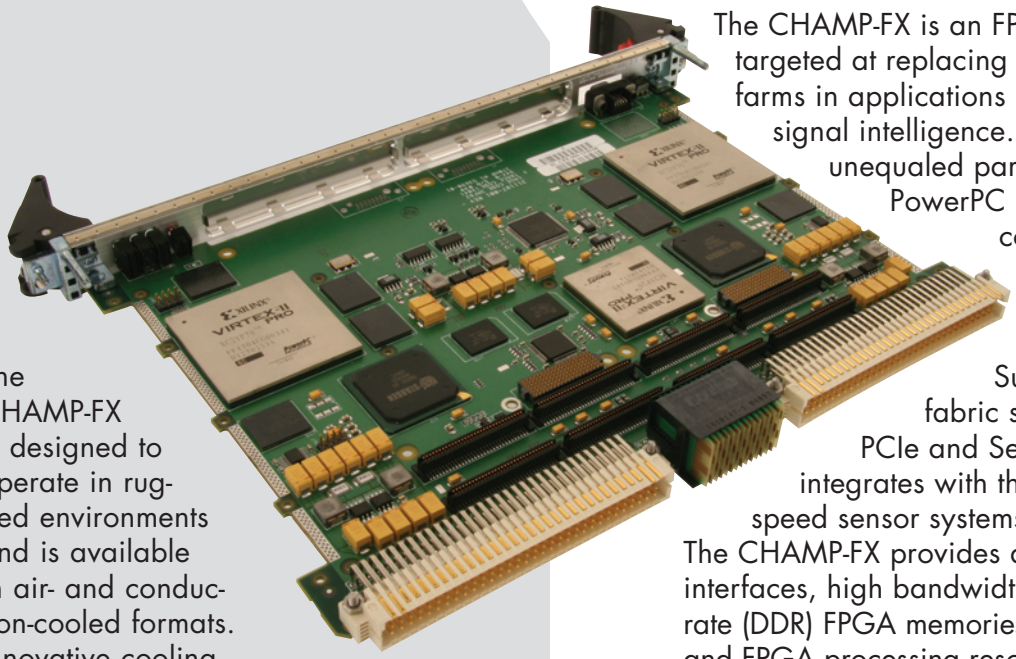
CHAMP-FX, FPGA Compute Engine



The CHAMP-FX is an FPGA computing platform targeted at replacing DSP, ASIC or processor farms in applications such as radar, sonar, and signal intelligence. FPGA technology allows unequaled parallelism, often outperforming PowerPC processors by 10x in terms of computing power by volume and power. The computing power is matched with ultra-high I/O bandwidth. Supporting the VITA-41 switch fabric standard with options for PCIe and Serial RapidIO, the CHAMP-FX integrates with the coming generation of high-speed sensor systems and DSP processing boards. The CHAMP-FX provides a balanced mix of mezzanine interfaces, high bandwidth I/O, numerous double data rate (DDR) FPGA memories, off-board fabric connectivity and FPGA processing resources. The 6U VME compatible card features two Xilinx Virtex-II Pro platform FPGAs (XC2VP70 orXC2VP100). The card architecture allows a flexible standalone or system-level platform for solving a variety of signal processing challenges. The CHAMP-FX has the ability to measure board temperatures and power dissipation of each FPGA. A flexible FPGA configuration manager allows each user FPGA to be easily loaded with configuration bit files stored on-board or via commands from a remote node or the on-board serial port.

The CHAMP-FX is designed to operate in rugged environments and is available in air- and conduction-cooled formats. Innovative cooling techniques are employed to handle high performance FPGA implementations. Curtiss-Wright provides an FPGA design kit to simplify and speed the development of FPGA-based systems. See the CHAMPtools-FX datasheet on our website for details.

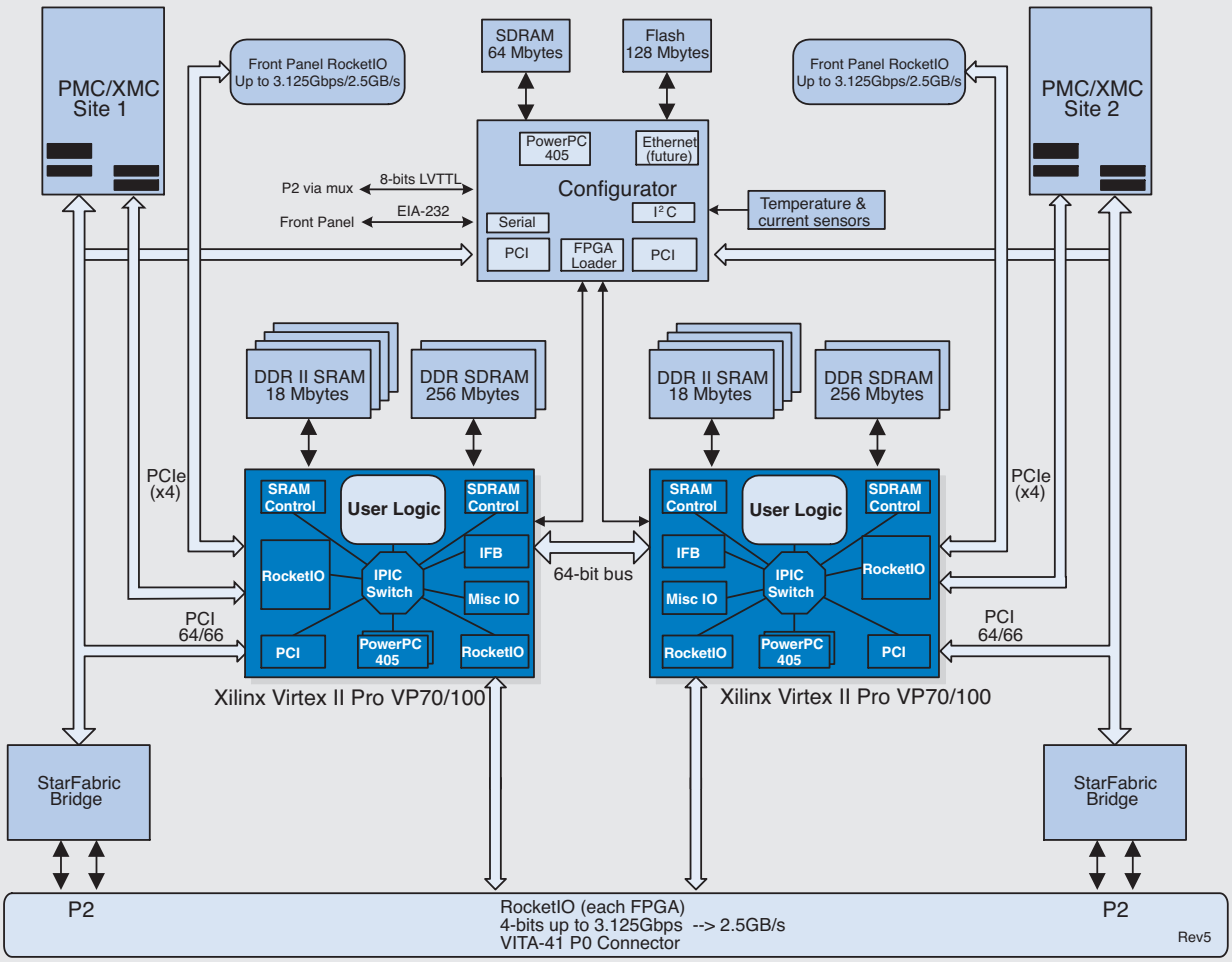
For more information on our broad range of high-integrity computing solutions, please visit our website at **www.cwcembedded.com**.

CURTISS WRIGHT Controls
Embedded Computing

CHAMP-FX, FPGA Compute Engine

Features

- Two user-programmable Xilinx Virtex-II Pro™ Platform FPGAs (XC2VP70 or XC2VP100)
- 512 Mbytes DDR-266 SDRAM
- 36 Mbytes DDR II SRAM, 4 separate banks per FPGA
- 64-bit inter-FPGA bus sustaining >1GB/s between FPGAs
- Two IBM 405 PowerPC processors within each FPGA
- Two PMC/XMC sites support 64-bit, 66MHz PCI, and VITA 42.2, 42.3 high-speed serial standards via 4-bit RocketIO interface
- PMC sites support Processor PMCs
- Backplane fabric support with VITA-41 P0 connector with two 4-bit, RocketIO ports. Total bi-directional bandwidth up to 5 GB/s
- VME64x with 95-pin P0 and VITA 41 versions available
- Front panel RocketIO connectors with two 4-bit, RocketIO ports Total bi-directional bandwidth up to 5 GB/s
- Two StarFabric interfaces, up to 880 MB/s aggregate data rate
- 128 Mbytes Flash for FPGA bit files and processor code
- On-board configurator FPGA manages boot-up, initialization, PCI bus enumeration, Flash file management and FPGA configuration
- EIA-232 serial port per FPGA for command and debug interface
- Thermal sensors for monitoring board temperatures
- Sensors for monitoring FPGA power consumption
- Support for ChipScope Pro and JTAG processor debug interfaces
- FPGA design kit with VHDL libraries, development environment, reference designs, simulation test benches and software libraries
- Range of air- and conduction-cooled ruggedization levels available



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