Data Sheet

CHAMP-AV8

2nd Generation Intel® Core™ Multi-processor OpenVPX™ Card

VPX™ VPX REDI™ OpenVPX™

Features

- Two Intel® Core™ i7-2715QE quad-core processors at up to 2.1 GHz
- AVX 256-bit floating-point vector unit
- Hyper-threading technology
- Up to 269 GFLOPs peak computing performance
- 4 Gbytes DDR3 SDRAM with ECC per processor, growth to 8 Gbytes
- 8 GB NAND flash per processor
- Protected backup boot flash
- 256 Kbytes NVRAM
- Secure write-protection on all non-volatile memory
- De-classify function to erase non-volatile memory
- Trusted Platform Management (TPM)
- PCI Express® (PCIe) local fabric with 2 GB/s bi-directional inter-processor bandwidth
- Gen2 Serial RapidIO® (sRIO) Data Plane interface, 8 GB/s bi-directional bandwidth
- Onboard Gen2 sRIO switch
- Gen 2 PCIe Expansion Plane interface on P2, up to 8 GB/s bidirectional bandwidth
- Eight channel PCIe DMA controller to off-load CPUs
- Two 1000Base-T Ethernet interfaces
- Two 1000Base-BX Ethernet interfaces
- One XMC mezzanine site
- Four EIA-232 serial ports
- Two EIA-422 serial ports
- Three USB 2.0 interfaces
- Two SATA interfaces
- 16 LVTTL I/O signals with interrupt
- Differential discrete I/O
- 12 general purpose timers
- Avionics watchdog timer
- 16 semaphore registers
- Multi-board synchronous clock feature
- Intelligent Platform Management Interface (IPMI) support
- Power consumption sensors
- Temperature sensors
- User variable processor frequency to control power consumption
- Continuum Software Architecture firmware
- VxWorks® BSP supporting SMP
- Linux (based on Fedora distribution)
- Continuum Vector AVX/SSE optimized DSP function library
- Continuum Insights multi-processor development tools
- Continuum IPC inter-processor communications library
- VITA 48 1" pitch
- VITA 65 compliant per MOD6-PAY-4F1Q2U2T-12.2.1 12

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Overview

The CHAMP-AV8 combines the floating-point performance of the latest 2nd generation Intel® Core™ processors with the substantial bandwidth and system-enabling features of the 6U OpenVPX™ form factor. Utilizing a pair of 2.1 GHz quad-core processors featuring the Advanced Vector Extensions (AVX) instruction set, the CHAMP-AV8 delivers up to 269 GFLOPs. The high-performance cores are kept working efficiently with three levels of internal cache and a 21 GB/s (peak) DDR3 memory sub-system connected directly to the processor.

The CHAMP-AV8 incorporates the enhancements of the OpenVPX (VITA 65) standard with a complete suite of Data Plane, Expansion Plane and Control Plane interfaces. With up to 32 GB/s of fabric performance, the CHAMP-AV8 has the bandwidth required to effectively harness the power of the processors.

The CHAMP-AV8 is supported with operating systems and development tools including VxWorks®, Linux®, and Gedae®. Curtiss-Wright Controls Embedded Computing provides signal processing libraries and a high-performance Inter-Processor Communications (IPC) Library for message passing and bulk data transfers. The Continuum Insights suite of multi-processor development tools provides system management, development, debugging and fabric analysis features to lower the cost of developing multi-core, multi-processor software.

Quad-Core Intel Core i7-2715QE Processors

The CHAMP-AV8 incorporates two Intel Core i7-2715QE quad-core processors which are a low power embedded implementation of micro-architecture codename Sandy Bridge. A major advancement for DSP applications is the introduction of the 256-bit AVX floating-point instructions. The AVX vector unit is backwards compatible with SSE instructions and doubles the peak floating-point performance over the previous generation. At 2.1 GHz, the Core i7-2715QE processor provides a peak 135 GFLOPS. Featuring a dual-channel, 1333 MHz DDR3 SDRAM interface, each CPU has a peak memory bandwidth of 21 GB/s. The 2nd generation Core processor features many improvements in the cache subsystem designed to increase hit-rate and lower latency. Each core contains first-level instruction and data caches (32 KB, 4-way) and a second-level unified cache (256 KB, 8-way). A large third level cache (6 MB 16-way) is shared between all processor cores. The Core i7-2715QE features Intel's Hyper-Threading technology which enables each core to execute two software threads concurrently. Hyper-Threading results in a higher utilization rate of the CPU execution units and thus a greater rate of instructions per unit of time.

OpenVPX Data Plane, Expansion Plane and Control Plane interfaces

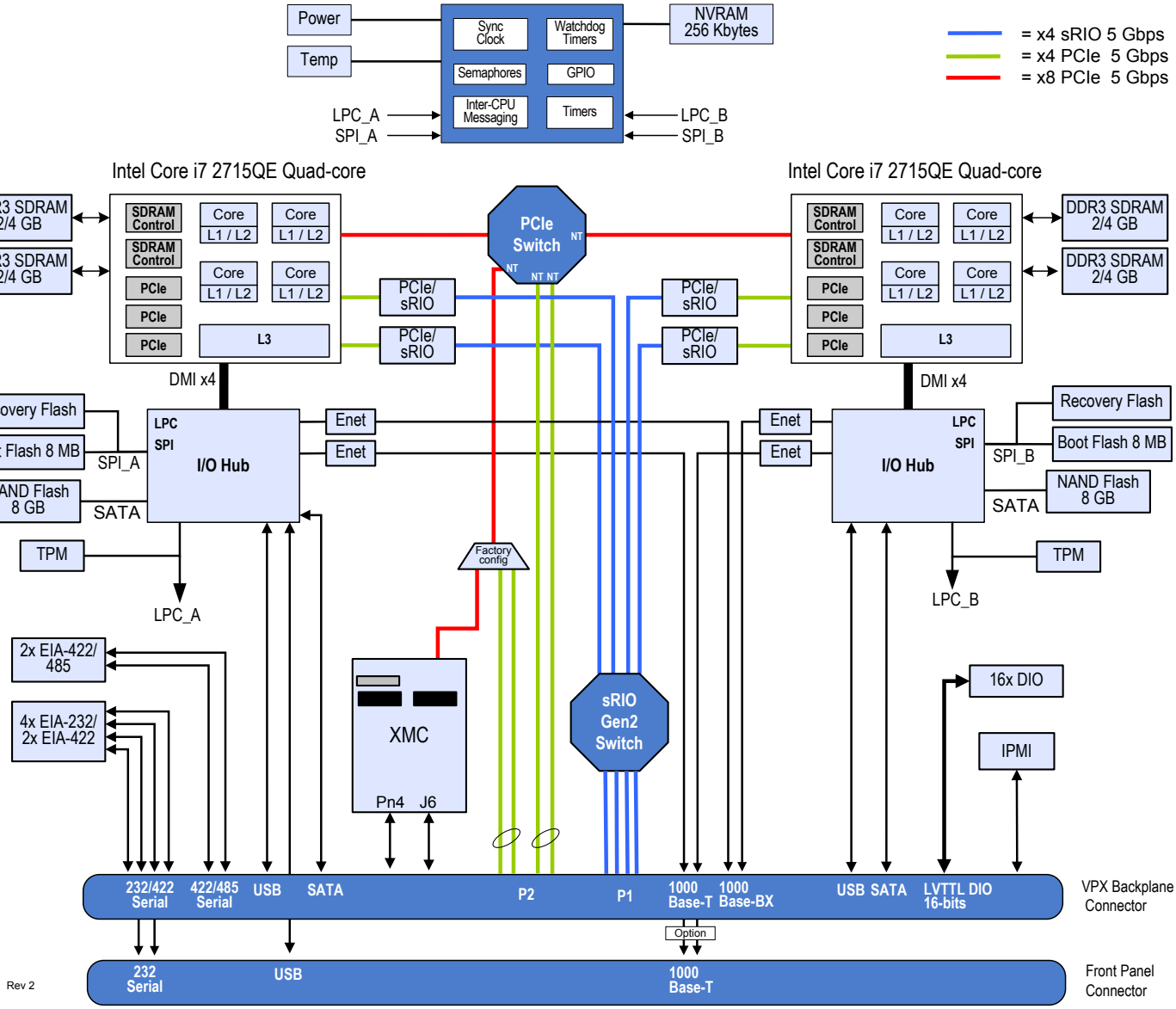
The OpenVPX (VITA 65) standard introduced the terminology of Data Plane, Expansion Plane, and Control Plane to describe the various high-speed serial interfaces that may be supported on VPX modules. The CHAMP-AV8 is equipped with a full implementation of these interfaces, providing:

- Data Plane: Gen2 sRIO on the P1 connector
- Expansion Plane: Gen2 PCIe on the P2 connector
- Control Plane: Gigabit Ethernet on the P4 connector

Serial RapidIO Data Plane Architecture

For the first time, the CHAMP-AV8 combines the computing performance of the latest Intel processors with the performance and power advantages of the sRIO fabric. The CHAMP-AV8 employs the new IDT PCIe to sRIO bridge component, bridging between Gen2 PCIe and Gen2 sRIO (5 Gbps). The sRIO bridge is fully featured with support for both memory-mapped transfers and sRIO messaging. The bridge also features multiple DMA channels with striding support to off-load the processors. Each processor is equipped with one or two PCIe/sRIO bridges, providing up to 8 GB/s bi-directional bandwidth at the board level, more than six times the performance of a 10 GbE interface with near-zero processor overhead. The CHAMP-AV8 also incorporates an IDT CPS-1848 Gen2 sRIO switch. The switch is connected to the processors via the PCIe-sRIO bridges and four ports on the Data Plane connector. The sRIO switch enables CHAMP-AV8 systems to employ either distributed switch, or centralized switch architectures. Distributed switch systems (example VITA 65 BPK6-CEN05-11.2.5-n backplane profile) make use of the local sRIO switch and thus avoid the need for a separate switch card. Larger systems typically use a centralized switch (example VITA 65 BPK6-CEN16-11.2.2-n backplane profile) such as the Curtiss-Wright VPX6-6902 sRIO/Ethernet switch.

Figure 1: CHAMP-AV8 Block Diagram





PCIe Express Data Plane Architecture

The CHAMP-AV8 makes use of the PCIe interfaces included in the CPU to share and transfer data between the processors, between cards via the P2 Expansion Plane connectors, and to communicate with the XMC site. Each processor connects with an onboard PCIe switch via an 8-lane Gen2 PCIe interface. The PCIe switch features non-transparent ports allowing each processor a full memory map, and access to the memory of the other processor. The CHAMP-AV8 presents two PCIe ports to the P2 expansion plane connector to form connections to I/O devices and/or other CHAMP-AV8 cards. See Table 1, Expansion Plane Interface Build-Time Options for details. Due to the non-transparent ports in the switch, there are no limitations due to multiple root complexes within the PCIe network. The PCIe switch features a four-channel DMA controller. The DMA offloads data movement overhead from the processors and is typically used to move data between processors and to/from the XMC and/or Expansion Plane devices. The DMA controllers operate from a descriptor queue in memory and features source and destination address striding, to facilitate data reorganization needs.

Table 1: CHAMP-AV8 Expansion Plane Configuration Options

XMC	P2 EP00-EP03	P2 EP04-EP07	P2 EP08-EP11	P2 EP12-EP15
x8	x4	x4	N/C	N/C
x8	x8		N/C	N/C
x4	x4	x4	x4	N/C
x4	x8		x4	N/C
N/C	x4	x4	x4	x4
N/C	x8		x8	

Notes
1. The EPxx references are from the VITA 65 specification which defines the mapping of x4/x8/x16 ports to the P2 connector. The CHAMP-AV8 does not support any x16 configurations.
2. The standard product configuration will be XMC x8 EP7-EP0 x8, EP15-8 N/C. Contact the factory for other configurations
3. N/C = No connection

Double Data Rate (DDR3) SDRAM with ECC

Each processor on the CHAMP-AV8 supports up to 8 Gbytes of DDR3 SDRAM for a total of 16 Gbytes on the board. (H1 2012 estimated for 16 GB support) The Core i7 2715QE processor features two independent memory controllers. With two banks of DDR3-1333 SDRAM, each processor achieves a peak memory bandwidth of over 21 GB/s. The memory is protected with Error Checking and Correcting (ECC) circuitry that can detect and correct all single-bit errors and detect all double-bit errors.

Protected Boot Flash Memory

Each processor is equipped with 8 Mbytes of flash memory used to store the system BIOS and Power-on diagnostics firmware (PBIT). In the event of accidental corruption of the primary boot flash, the CHAMP-AV8 is fitted with secondary boot flash devices. By application of a hardware jumper, or assertion of a backplane signal, the processors will boot from the secondary flash to regain operation of the card and recovery of the primary flash. Both primary and secondary boot flash devices feature hardware write-protection jumpers.

NAND Flash Memory

The CHAMP-AV8 features 8 Gbytes of NAND flash per processor (16 Gbytes total) for storage of the operating system and user application software. The NAND flash is interfaced to the processor via a SATA interface. Software access to the flash is via the operating system file system. An integrated flash controller implements bad block management and wear leveling functions. For maximum reliability and longevity, Single Level Cell (SLC) technology flash devices are used. Hardware jumpers are provided to disable write access to the NAND flash.

Non-volatile RAM (NVRAM)

A 256 Kbyte non-volatile memory based on ferroelectric technology (FRAM) provides non-volatile storage of mission state data that must not be lost when power is removed. During normal operation, application software reads and writes (via BSP function) the serial NVRAM which behaves like an SRAM, except that data is retained after power is removed. Both processors have access to the NVRAM device. Data written to the NVRAM is immediately non-volatile. The device is rated for a minimum of 100 Trillion (1014) read/write cycles. The data retention period is >10 years. For security against inadvertent writes to NVRAM, a hardware write-protection feature is provided.



Non-volatile Memory Security

The CHAMP-AV8, like other Curtiss-Wright Continuum Architecture products, provides for the management of non-volatile memory devices in classified circumstances. All of the non-volatile devices, boot flash, backup boot flash, NAND flash, NVRAM and FPGA PROM may be write-protected by hardware jumpers. The jumpers may be visually inspected to conform to security procedures.

The firmware of the CHAMP-AV8 provides a non-volatile memory scrub function to perform a secure erase of the boot flash, NAND flash and NVRAM per NISPOM requirements.

Gigabit Ethernet

Each processor on the CHAMP-AV8 is equipped with two Gigabit Ethernet interfaces. One interface conforms to 10/100/1000Base-TX (4-pair, transformer-coupled). The 1000Base-TX ports are available at the front panel or backplane connector as a build-time option. The other interface supports 1000Base-BX, also known as SerDes Ethernet. The 1000Base-BX interfaces are elements of the VITA 65 specification. The 2-pair AC-coupled signals are designed to support backplane connections to a local in-system Ethernet switch such as the Curtiss-Wright VPX6-6902 sRIO/Ethernet switch.

XMC Mezzanine Site

The CHAMP-AV8 is equipped with one mezzanine site supporting VITA 42.3 XMC modules. The mezzanine site is supported with an 8-lane PCIe interface providing up to 2 GB/s transmit and 2 GB/s receive simultaneously. The mezzanine site is enumerated and interrupt managed by Processor A, but can send/receive data to/from either processor via the PCIe switch. Note that the processor and switch support Gen2 PCIe speeds, but the VITA 42 designated connector is rated only for Gen1 speed. The XMC site provides Pn4 and Pn6 connectors for I/O to the VPX backplane connectors. The Pn6 I/O confirms to the VITA 46.9 P5w3P6-X38s+X8d+X12d mapping, supporting 20 differential pairs and 38 single-ended signals to the P5 and P6 connectors per rule 5-12. The Pn4 I/O conforms to the VITA 46.9 P3w1-P64s mapping, supporting 64 single-ended signals to the P3 connector per rule 5-2.

The CHAMP-AV8 supplies 12 V to the XMC VPWR pins, and 3.3 V up to a maximum of 4 A each.

Utility Features, Semaphores and Timers

The CHAMP-AV8 features a number of utility features to facilitate multi-processor application software.

The board provides sixteen hardware semaphore registers which are useful to coordinate the sharing of hardware resources between multiple tasks. The hardware solution provides a faster alternative to traditional software/memory techniques and avoids the use of shared memory to access the semaphores.

The CHAMP-AV8 provides six general purpose 32-bit timers. These may be configured for a timeout value between 20ns and 85sec, with a resolution of 20ns. Each timer may be configured to generate an interrupt to either processor. The current timer value may be read at any time by software. Note that up to two timers may be reserved to support operating system features.

Avionics Style Watchdog Timer

The CHAMP-AV8 provides two watchdog timers for each processor. Each watchdog timer is a pre-settable down-counter with a resolution of 1 µsec. Time-out periods from 0 ms to 33.6 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, a backplane signal can be asserted to disable all watchdog interrupts.

The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can be configured to operate in "Avionics" mode whereby a minimum interval between writes to the watchdog register is also enforced. Writing to the watchdog register too soon or too late causes an exception event.

Multi-board Synchronous Clock

The CHAMP-AV8 includes a special purpose counter which may be synchronized with corresponding counters on other boards in the same system. This common time base allows a developer to time-stamp messages and/or data buffers, with the knowledge that the local time is maintained at the



same value by all the boards in the system. The counter can be set to roll-over to a pre-load value and interrupt on roll-over. This feature is typically most valuable for debugging and instrumenting multi-board applications code, which can present challenges in coordinating the distribution of data items between processors.

Serial Ports

The CHAMP-AV8 provides four EIA-232 serial ports and two EIA-422 serial ports.

Each processor has two EIA-232 serial ports, implemented with 16550-compatible UARTs within the Core Functions FPGA. The EIA-232 serial ports support asynchronous communications with one transmit and one receive signal. One port from each processor is available on the front panel connector. Both ports from each processor are connected to the backplane connectors. The EIA-232 ports support operation up to 115 Kbaud.

Each processor is provided with an EIA-422/485 differential serial port utilizing a 16550-compatible UART within the Core Functions FPGA. The EIA-422/485 ports support asynchronous communications with one transmit and one receive pair each. The EIA-422/485 ports are connected to the backplane connectors. The EIA-422 ports support operation up to 115 Kbaud.

USB and SATA Interfaces

The CHAMP-AV8 has a total of three external USB 2.0 interfaces. Both processors have a USB interface routed to the backplane connector. Processor A has an additional USB interface routed to the front panel connector. A current-limited USB power supply is provided for each interface.

Each processor has an eSATA interface to the backplane connector.

LVTTL Discrete Digital I/O

The CHAMP-AV8 provides 16 general purpose LVTTL I/O lines which are accessible at the backplane connector. Each bit is individually programmable to be an input, output or I/O. All bits configured as an input may be used to trigger an interrupt which is further programmable to be level or edge sensitive. Both levels and transition directions may be detected. The LVTLL I/O lines are terminated with an onboard pull-up resistor. The digital I/O lines are 5 V tolerant.

EIA-422 Differential Discrete Digital I/O

The CHAMP-AV8 provides the capability to discretely control the outputs of the two EIA-422 drivers which are normally associated with EIA-422 serial channels. In a similar fashion, there are registers that can read the state of the EIA-422 receivers, independent of the serial controller. In total there are two inputs and two outputs. The inputs may be configured to generate an interrupt. When configured as discrete differential I/O, the drivers and receivers can be used as general-purpose differential-mode control signals unrelated to serial I/O.

Power and Temperature Sensors

The CHAMP-AV8 is equipped with a suite of power and temperature sensors that provide users with an unprecedented visibility into the environmental conditions encountered by the card. The card features current and voltage sensors for the backplane power rails, enabling the user to measure the real-time power consumption of the entire card. The measured power includes 12 V power consumed by installed mezzanine modules. Since the power consumption of the board depends on many factors—including the processor clock frequency, the nature of the software, SDRAM loading, and the operating temperature of the card— the ability to measure actual power for a given application eliminates guesswork in system power consumption estimates.

The CHAMP-AV8 also provides a number of temperature sensors. There are sensors for the edges and center of the board, the processor die, and Platform Controller Hub (PCH) die.

Indicator LEDs

The CHAMP-AV8 provides eight user-controllable green LEDs, four per processor. These are visible on the front panel. There is an additional red LED on the front panel to indicate a failure determined by the onboard diagnostic firmware. A backplane signal is also asserted in conjunction with the fail LED.

Operating System Software

The CHAMP-AV8 is supported with an extensive array of software, which cover all facets of developing application code for the board. Users have the option of choosing



to develop with a variety of operating systems and development tools. The following operating systems are supported on the CHAMP-AV8:

- VxWorks 6.x, Workbench 3.x from Wind River (Part number DSW-462-000-VXW)
- Linux Software Development Kit. Based on Fedora Distribution, formally termed Fedora Remix (Part number DSW-462-002-LNX). Note that the drivers contained in the Linux SDK may be integrated by the user with other Linux environments such as Red Hat.

Continuum IPC Library

continuum
INTER-PROCESSOR COMMUNICATIONS

The Continuum Inter-Processor Communications Library (IPC) is a library of functions designed to enable high-performance, low-latency message passing. IPC allows processors to communicate task-to-task, on the same card over local interconnect, or between boards over a system level interconnect. IPC supports several transport mechanisms including PCI/PCIe, StarFabric and sRIO. Applications developed on CHAMP-AV2/3/4/5/6 or SVME/DMV-183/184/185 will port to the CHAMP-AV8 with no changes related to the IPC layer.

Continuum IPC provides low-overhead block data transfers, segmented block data transfers and signaling between processors to assist in high-bandwidth data movement. See the Continuum IPC Library datasheet for more details.

Continuum Vector Library

continuum
VECTOR

The CHAMP-AV8 derives its floating-point performance from the Intel AVX vector processing unit. The Continuum Vector Library provides over 200 functions optimized for the AVX/SSE unit, providing the foundation for most signal processing applications. Continuum Vector provides the user with a choice of APIs with support for the Vector Signal Image Processing Library (VSIPL, Core Lite) standard and the popular API established by Floating Point Systems Inc. See the Continuum Vector datasheet for detailed information.

Continuum Insights

continuum
INSIGHTS

The Continuum Insights visualization and instrumentation tools are designed to ease and optimize the development of application software for multi-computer embedded systems. The Insights suite of tools is based on the Eclipse™ Development and Application Framework, and includes an Event Analysis Tool, a System Monitoring Tool and System Management Functions. See the Continuum Insights datasheet for detailed information.

The Event Analysis tool provides an extension to the Wind River System Viewer tool to provide a post run-time view of time-correlated events across multiple processors in a system. The Event Analysis tool greatly simplifies the process of testing, verifying and debugging complex multiprocessor software.

The System Monitoring tool provides a hierarchical, graphical representation of a system of VPX boards. Chassis, board and processor views present dozens of hardware and software information items with real-time updates of processing thread, utilization, task allocation and other status information such as board temperatures.

The System Management tool automates the startup of a multi-computer with user libraries and executables. The tool manages the contents of all flash devices in a system, individually or in defined groups. Users can work with multiple targets simultaneously, using a facility to group telnet sessions to a single console with color coding and interleaving for easy delineation.

The Continuum Insights multi-processor debugger tool extends the capabilities of the Wind River Workbench debugger, enabling the debugging facilities to be used on many processors simultaneously. The debugger also allows break points to be set up in such a way that when a break point occurs on one of the processors in the system, all user tasks on the other processors are suspended. This eliminates problems that can occur otherwise when running processors interfere with the processor that has hit a breakpoint.

Cables and Rear Transition Modules

The CHAMP-AV8 features a high-density front panel connector. The connector provides access to two EIA-232 serial ports, 2 GbE ports, one USB port, and a board reset input. A cable is available (part number CBL-462-FPL-000) that breaks out the signals to a number of standard connectors.

A Rear Transition Module (RTM) is available (part number RTM-462-000) to provide easy access to the backplane I/O signals. The RTM is a 6Ux80mm (1101.10 compliant)



module, with a rear face plate and injector/ejector handles that plugs into the rear of the VPX backplane to make connections with the I/O signals emanating from the CHAMP-AV8 connectors. The RTM in conjunction with an included break-out cable provides connectors for 1000Base-T GbE (2), EIA-232 (4), EIA-422/485 (2), USB (2) and SATA (2).

The RTM also features a number of switches and headers for access to other CHAMP-AV8 signals and I/O ports. The RTM is intended for development purposes and is not tested or warranted for shock and vibration.

Ordering Information

The CHAMP-AV8 is ordered with the following part numbers:

Table 2: Part Numbers

VPX6-462-UVWXYYY	
U	Cooling method A: air-cooled C: conduction-cooled F: air flow through
V	Temperature range 0: 0°C to 50°C 1: -40°C to 71°C 2: -40°C to 85°C
W	Mechanical format 4: 1" pitch
X	Backplane fabric configuration A: 4 sRIO on P1, XMC NC, EP00-EP07 x8, EP08-15 x8 B: 4 sRIO on P1, XMC x8, EP00-EP07 x8, EP08-15 NC C: 4 sRIO on P1, XMC x4, EP00-EP07 x8, EP08-11 x4
YYY	Identifies a specific configuration that typically describes processor speed, memory and other configurable options

Note:
1. A formal quote from Curtiss-Wright or authorized representative will provide a complete part number and description of the configuration
2. The CHAMP-AV8 IPMI feature is optional. Contact the factory for further information.
3. Contact the factory for air flow through inlet temperature and CFM specifications

Ruggedization Levels

Air-cooled cards are available in Levels 0.

See the Curtiss-Wright Ruggedization Guidelines factsheet for more information.

Table 3: Dimensions and Weight

Option	Dimensions	Weight
Air-cooled Level 0	per VITA 48, 1" pitch (note 1)	<1000g (estimated)
Air-cooled Level 100	per VITA 48, 1" pitch (note 1)	<1100g (estimated)
Conduction-cooled	per VITA 48, 1" pitch (note 1)	<1250g (estimated)

Note:
Front panel hardware on air-cooled modules includes: injector/extractor handles, EMC strip, alignment pin, and keying provisions in accordance with ANSI/VITA 1.1, American National Standards for VME64 Extensions (and IEEE 1101.10).

Table 4: Power Requirements

Backplane Power Rail	Usage
12 V (Vs1)	Used for main power (see note)
3.3 V_Aux	Used for IPMI controller power
12 V_Aux	Optional. Used for XMC power
-12 V_Aux	Optional. Used for XMC power

Note:
The CHAMP-AV8 power consumption will vary depending on processor frequency, application usage and ambient temperature. Consult the user manual or factory for power characterization information

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

Technical Support

For technical support:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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