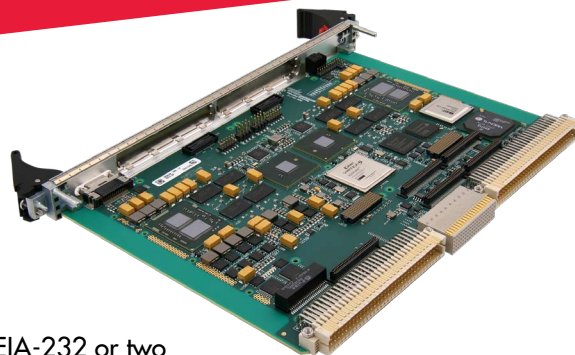Data Sheet

# CHAMP-AV5
## VME64x Dual-core Core™ i7 DSP Board

## Features

- Two Intel® Dual-core Core™ i7 processors at up to 2.53GHz
- SSE 4.2 floating point vector unit
- Hyper-threading technology
- Pin-compatible upgrade for CHAMP-AV4 systems
- Up to 81GFLOPs peak computing performance
- 2GB DDR3 SDRAM with ECC per processor
- 8GB NAND FLASH on SATA per processor
- Protected backup boot FLASH
- 256KB NVRAM
- Secure write-protection on all non-volatile memory
- De-classify function to erase non-volatile memory
- Trusted Platform Management (TPM)
- PCI Express® (PCIe) local fabric with up to 4GB/s aggregate inter-processor bandwidth
- Four channel PCIe DMA controller to off-load CPUs
- Gigabit Ethernet (1000Base-T) per processor
- Two mezzanine sites
- One XMC/PMC (PCIe x4, 100MHz PCI-X)
- One XMC (PCIe x8)

- Four EIA-232 or two EIA-422/485 serial ports
- Three USB 2.0 interfaces
- One external SATA port
- Eight LVTTL I/O signals with interrupt
- Differential discrete I/O
- 12 general purpose timers
- Avionics watchdog timer
- 16 semaphore registers
- Multi-board synchronous clock feature
- Power consumption sensors
- Temperature sensors
- User variable processor frequency to control power consumption
- VME64x, 2eVME, and 2eSST protocols
- Continuum Software Architecture firmware
- VxWorks® BSP supporting SMP
- Wind River® Linux®
- Continuum Vector™ SSE optimized DSP function library

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## Overview

The CHAMP-AV5 multi-processing board brings the floating point performance of the Intel Core i7 architecture to VME64x form factor standard. Utilizing a pair of 2.53GHz dual-core Core i7 processors, the CHAMP-AV5 delivers up to 81 GFLOPs of performance.

The CHAMP-AV5 features a high-bandwidth PCIe architecture, featuring on-board PCIe connections between the processors, and the PMC/XMC sites. With 8GB of FLASH and 4GB of SDRAM the CHAMP-AV5 handles applications with demanding storage, data logging and sensor processing needs. The CHAMP-AV5 is pin-compatible with the MPC7447/7448-based CHAMP-AV4 allowing for performance upgrades without changing chassis, backplane, power supplies of existing qualified systems. The CHAMP-AV5 is supported with an extensive suite of software including support for VxWorks and Linux, Inter-processor communication and the Continuum Vector SSE-optimized signal processing library.

## Dual-core Intel Core i7 Processors

The CHAMP-AV5 incorporates two Intel Core i7 dual-core processors. The Core i7 610e device is a low power implementation of the Nehalem family of processors. The performance of the processor for DSP applications is aided by the introduction of integrated memory controllers. Featuring a dual-channel, 1066MHz DDR3 SDRAM interface, each CPU has a peak memory bandwidth of 17GB/s. A major performance improvement of the Core i7 architecture is the three-level cache subsystem. Each core contains first-level instruction and data caches (32KB, 4-way) and a second-level unified cache (256KB, 8-way). A large third level cache (4MB 16-way) is shared between both processor cores. The Core i7 610e features Intel's Hyper-Threading Technology which enables each core to execute two software threads concurrently. Hyper-Threading results in a higher utilization rate of the CPUs execution units and thus a greater rate of instructions per unit of time. Even in the highly floating point intensive SPECFP benchmark, the addition of the virtual Hyper-Threaded cores resulted in a 7% performance improvement. Each core is equipped with the Intel Streaming SIMD Extensions (SSE 4.2) vector processor unit. The 128-bit SSE registers can process both single and double-precision formats with up to eight floating point operations per cycle.

## PCI Express Architecture

The CHAMP-AV5 makes use of the PCIe interface included in the Core i7 CPU to share and transfer data between the processors and to communicate with the XMC/PMC sites. The card features a local PCIe switch to connect the processors and XMC/PMC sites in a high-speed fabric. Each processor is equipped with an 8-lane interface to the switch, providing a 2GB/s transmit and 2GB/s receive data path between the two processors. The PCIe switch features non-transparent ports allowing each processor a full memory map, and access to the memory of the other processor. The PCIe switch also features a four channel DMA controller. The DMA off-loads data movement overhead from the processors and is typically used to move data between processors and to/from the XMC/PMC devices. The DMA controllers operate from a descriptor queue in memory and feature source and destination address striding to facilitate data reorganization needs.

## Double Data Rate (DDR3) SDRAM with ECC

Each processor node on the CHAMP-AV5 supports 2GB of DDR3 SDRAM for a total of 4GB on the board. The Core i7 processor features two independent memory controllers. With two banks of DDR3-1066 SDRAM each processor achieves a peak memory bandwidth of over 17GB/s. The memory is protected with Error Checking and Correcting (ECC) circuitry that can detect and correct all single-bit errors and detect all double-bit errors.

## Protected Boot FLASH Memory

Each processor is equipped with 8MB of FLASH memory used to store the system BIOS and Power-on diagnostics firmware (PBIT). In the event of accidental corruption of the primary boot FLASH, the CHAMP-AV5 is fitted with secondary boot FLASH devices. By application of a hardware jumper, or assertion of a backplane signal, the processors will boot from the secondary FLASH to regain operation of the card and recovery of the primary FLASH. Both primary and secondary boot FLASH devices feature hardware write-protection jumpers.

## NAND FLASH Memory

The CHAMP-AV5 features 8GB of NAND FLASH per processor (16GB total) for storage of the operating system and user application software. The NAND FLASH is interfaced to the processor via a SATA interface. Software

access to the FLASH is via the operating system file system. The on-board FLASH controller implements bad block management and wear leveling functions. For maximum reliability and longevity, Single Level Cell (SLC) technology FLASH devices are used. Hardware jumpers are provided to disable write access to the NAND FLASH.

## Non-Volatile RAM (NVRAM)

A 256KB non-volatile memory based on ferroelectric technology (F-RAM) provides non-volatile storage of mission state data that must not be lost when power is removed. During normal operation, application software reads and writes the NVRAM just like a standard SRAM except that data is retained after power is removed. Both processors have access to the NVRAM device. Data written to the NVRAM is immediately non-volatile. The device is rated for a minimum of 100 Trillion ($10^{14}$) read/write cycles. The data retention period is >10 years. For security against inadvertent writes to NVRAM, a hardware write-protection feature is provided.

## Non-volatile Memory Security

The CHAMP-AV5, as well as other Curtiss-Wright Controls Continuum Architecture products, provides for the management of non-volatile memory devices in classified circumstances. All of the non-volatile devices, boot FLASH, backup boot FLASH, NAND FLASH, NVRAM and FPGA PROM may be write-protected by hardware jumpers. The jumpers may be visually inspected to conform to security procedures.

The firmware of the CHAMP-AV5 provides a non-volatile memory scrub function to perform a secure erase per NISPOM requirements.

## Gigabit Ethernet

Each processor on the CHAMP-AV5 is equipped with a 10/100/1000Base-TX Gigabit Ethernet interface. The Ethernet ports are available at the front panel or backplane connector as a build-time option on air-cooled cards, and at the backplane connector on conduction-cooled cards.

## XMC/PMC Mezzanine Sites

The CHAMP-AV5 is equipped with two mezzanine sites. One site is capable of supporting either IEEE-1386 PMC or VITA 42.3 XMC modules. The other site supports XMC modules only. PMC modules with PCI or PCI-X interfaces ranging from 32-bit, 33MHz to 64-bit, 100MHz are supported. Legacy 5V-only PMC modules are not supported. Mezzanine cards may be controlled by either processor.

XMC modules are supported per the VITA 42.3 standard. The XMC-only site is equipped with an 8-lane PCIe interface providing up to 2GB/s transmit and 2GB/s receive simultaneously. The XMC/PMC site is equipped with a 4-lane PCIe interface. 4-lane XMC modules may be used in either site. The PMC/XMC sites provide Pn4 connectors for I/O to the P0 and P2 connectors. The I/O routing from Pn4 to P0 and P2 is implemented as 32 differential pairs and is compatible with the PMC-233 StarLink II StarFabric PMC module.

The conduction-cooled versions of the CHAMP-AV5 adhere to the IEEE 1386-2001 and ANSI/VITA 20-2005 standards for conduction-cooled PMCs. The CHAMP-AV5 thermal frame provides the best possible thermal interface for mezzanine modules by supporting the primary and secondary thermal interfaces. To support high-power modules, the CHAMP-AV5 thermal frame supports a mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed PMC/XMC modules can significantly lower the temperature rise between the CHAMP-AV5 card edge and the PMC/XMC components. The mid-plane thermal shunt does not impinge on the IEEE 1386-2001 specified component height.

## Utility Features, Semaphores, Timers

The CHAMP-AV5 features a number of utility features to facilitate multi-processor application software.

The board provides 16 hardware semaphore registers which are useful to coordinate the sharing of hardware resources between multiple tasks. The hardware solution provides a faster alternative to traditional software/memory techniques and avoids the use of shared memory to access the semaphores.

The CHAMP-AV5 provides six general purpose 32-bit timers. These may be configured for a timeout value between 20ns and 85sec, with a resolution of 20ns. Each timer may be configured to generate an interrupt to either processor. The current timer value may be read at any time by software. Note that up to two timers may be reserved to support operating system features.

## Avionics Style Watchdog Timer

The CHAMP-AV5 provides two watchdog timers for each processor. Each watchdog timer is a pre-settable down-counter with a resolution of 1 μsec. Time-out periods from 0ms to 33.6 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, a backplane signal can be asserted to disable all watchdog interrupts.

The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can be configured to operate in "Avionics" mode whereby a minimum interval between writes to the watchdog register is also enforced. Writing to the watchdog register too soon or too late causes an exception event.

## Multi-board Synchronous Clock

The CHAMP-AV5 includes a special purpose counter which may be synchronized with corresponding counters on other boards in the same system. This common time base allows a developer to time-stamp messages and/or data buffers, with the knowledge that the local time is maintained at the same value by all the boards in the system. The counter can be set to roll-over to a pre-load value and interrupt on roll-over. This feature is typically most valuable for debugging and instrumenting multi-board applications code, which can present challenges in coordinating the distribution of data items between processors.

## Serial Ports

The CHAMP-AV5 provides up to four serial ports which are user configurable to operate with EIA-232 or EIA-422/485 electrical interfaces. Two ports are available to each processor. The serial ports share a common group of pins on the backplane connector. When configured to operate in EIA-422/485 mode, one port utilizes the pins that are otherwise used by two EIA-232 ports. The following configurations are possible:

- Four EIA-232, two from each processor node.
- Two EIA-232 from processor node A and one EIA-422/485 from processor node B.
- One EIA-422/485 from processor node A and two EIA-232 from processor node B.
- Two EIA-422/485, one from each processor node.

In both EIA-232 and EIA-422/485 configuration, the ports support transmit and receive signals only. Internally the signals are routed through an FPGA which could optionally be configured to provide a synchronous capability. Consult the factory for more information.

All four ports are connected simultaneously to the front panel connector (air-cooled cards) and the backplane connector. The serial ports support asynchronous operation up to 115 Kbaud.

## USB and SATA Interfaces

The CHAMP-AV5 has a total of three external USB 2.0 interfaces. Both processors have a USB interface routed to the P2 connector. One processor has an additional USB interface routed to the front panel connector. A current-limited USB power supply is provided for each interface.

One of the processors is provided with a SATA interface to the P0 backplane connector.

## LVTTL Discrete Digital I/O

The CHAMP-AV5 provides eight general purpose LVTTL I/O lines which are accessible at the backplane connector. Each bit is individually programmable to be an input, output or I/O. All bits configured as an input may be used to trigger an interrupt which is further programmable to be

level or edge sensitive. Both levels and transition directions may be detected. The LVTLL I/O lines are terminated with an on-board pull-up resistor. The digital I/O lines are 5V tolerant.

## EIA-422 Differential Discrete Digital I/O

The CHAMP-AV5 provides the capability to control discretely, the outputs of the two EIA-422 drivers which are normally associated with EIA-422 serial channels. In a similar fashion, there are registers that can read the state of the EIA-422 receivers, independent of the serial controller. In total there are two inputs and two outputs. The inputs may be configured to generate an interrupt. When configured as discrete differential I/O, the drivers and receivers can be used as general-purpose differential-mode control signals unrelated to serial I/O.

## Power and Temperature Sensors

The CHAMP-AV5 is equipped with a suite of power and temperature sensors that provide users with an unprecedented visibility into the environmental conditions encountered by the card. The card features current and voltage sensors for the backplane power rails, enabling the user to measure the real-time power consumption of the entire card. The measured power includes 5V/3.3V power consumed by any installed mezzanine modules. Since the power consumption of the board depends on many factors including the processor clock frequency, the nature of the software, SDRAM loading, and the operating temperature of the card, the ability to measure actual power for a given application eliminates guesswork in system power consumption estimates.

The CHAMP-AV5 also provides a number of temperature sensors. There are sensors for the edges and center of the board, the processor die, the I/O hub die and the Core Functions FPGA die.

## Indicator LEDs

The CHAMP-AV5 provides four user-controllable green LEDs. These are visible on the front panel of air-cooled boards and visible on the back side of conduction-cooled boards. There is an additional red LED on the front panel of both versions to indicate a failure determined by the on-board diagnostic firmware. A backplane signal is also asserted in conjunction with the fail LED.

## VMEbus Interface

The CHAMP-AV5 is equipped with a VME master/slave interface. The interface is implemented with the Tundra Tsi148™ PCI/X to VME bridge. The Tsi148 supports the 2eSST VMEbus transfer protocol offering the maximum possible VME performance, while retaining full backwards compatibility with legacy VME systems. Both processor nodes of the CHAMP-AV5 can be mapped to have direct access to the VMEbus, or use the Tsi148 internal DMA engine to move between local memory and the VMEbus.

## Operating System Software

The CHAMP-AV5 is supported with an extensive array of software items, which cover all facets of developing application code for the board. Users have the option of choosing to develop with a variety of operating systems and development tools. The following operating systems are supported on the CHAMP-AV5.

VxWorks 6.x, Workbench 3.x from Wind River. (Part number DSW-417-000-VXW)

Wind River Linux Software Development Kit from Curtiss-Wright (Part number DSW-417-001-LNX)

## Continuum IPC™ Library

The Continuum Inter-Processor Communications (IPC) Library is a library of functions designed to enable high-performance, low-latency message passing. Continuum IPC allows processors to communicate task-to-task, on the same card over local interconnect, or between boards over a system level interconnect. Continuum IPC supports several transport mechanisms including PCI/PCIe, StarFabric and Serial RapidIO® (SRIO). Applications developed on CHAMP-AV2/3/4/6 or SVME/DMV-183/184/185 will port to the CHAMP-AV5 with no changes related to the Continuum IPC layer.

Continuum IPC provides low-overhead block data transfers, segmented block data transfers and signaling between processors to assist in high-bandwidth data movement. See the Continuum IPC Library datasheet for more details.

## Continuum Vector™ Library

The CHAMP-AV5 derives its floating-point performance from the Intel SSE 4.2 vector processing unit. The Continuum Vector Library provides over 200 functions optimized for the SSE unit, providing the foundation for most signal processing applications. Continuum Vector provides the user with a choice of APIs with support for the Vector Signal Image Processing Library (VSIPL, Core Lite) standard and the popular API established by Floating Point Systems Inc. See the Continuum Vector datasheet for detailed information.

## Cables and Rear Transition Modules

The CHAMP-AV5 features a high-density front panel connector on air-cooled versions of the board. The connector provides access to two EIA-232 serial ports, two Gigabit Ethernet ports, one USB port, and a board reset input. A cable is available, part number CBL-417-FPL-000 that breaks out the signals to a number of standard connectors.

A Rear Transition Module (RTM) is available (part number RTM-417-000) to provide easy access to the backplane I/O signals. The RTM is a 6U x 80mm (1101.10 compliant) module with a rear face plate and injector/ejector handles that plugs into the rear of the VME backplane to make connections with the I/O signals emanating from the CHAMP-AV5 P0 and P2 connectors. The RTM in conjunction with an included break-out cable provides connectors for Gigabit Ethernet (2), EIA-232 (4), EIA-422/485 (2), USB (2), SATA (1), StarFabric (4 RJ45s).

The RTM also features a number of switches and headers for access to other CHAMP-AV5 signals and I/O ports. The RTM is intended for development purposes and is not tested or warranted for shock and vibration.

## Ordering Information

The CHAMP-AV5 is ordered with the following part numbers. SVME-417-xyyy denotes air-cooled versions of the product, where "x" defines the ruggedization level, (0,1,2 etc.) and "yyy" identifies a specific configuration. DMV-417-xyyy denotes conduction-cooled versions of the product, following the same conventions. Note that a configuration may also include one or more installed PMC modules. A formal quote from Curtiss-Wright Controls or authorized representative will provide a complete part number and description of the configuration.

## Ruggedization Levels

Air-cooled cards are available in levels 0, 100.

Conduction-cooled cards are available in levels 100 and 200

See the Curtiss-Wright Controls Ruggedization Guidelines factsheet for more information.

## Specifications

### Table 1: Dimensions and Weight

| Option | Dimensions | Weight |
|---|---|---|
| Air-cooled | per ANSI/VITA 1-1994 (Note 1) | <570g (estimated) |
| Conduction-cooled | per IEEE 1011.2 (Note 2) | <750g (estimated) |

Notes:
1. Front panel hardware on air-cooled modules includes: injector/extractor handles, EMC strip, alignment pin, and keying provisions in accordance with ANSI/VITA 1.1, American National Standards for VME64 Extensions (and IEEE 1101.10).
2. Uses a full width thermal interface surface to maximize thermal performance which is a small deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in standard air-cooled chassis.

### Table 2: Power Requirements

| Volts | Usage |
|---|---|
| 5V | Used for main power (Note 1) |
| 3.3V | Used for main power (Note 1) |
| 12V | Used for XMC/PMC power |
| -12V | Used for XMC/PMC power |

Notes:
1. The CHAMP-AV5 power consumption will vary depending on processor frequency, application usage and ambient temperature. Consult the user manual or factory for power characterization information

## Figure 1: CHAMP-AV5 Block Diagram



Figure 1: CHAMP-AV5 Block Diagram
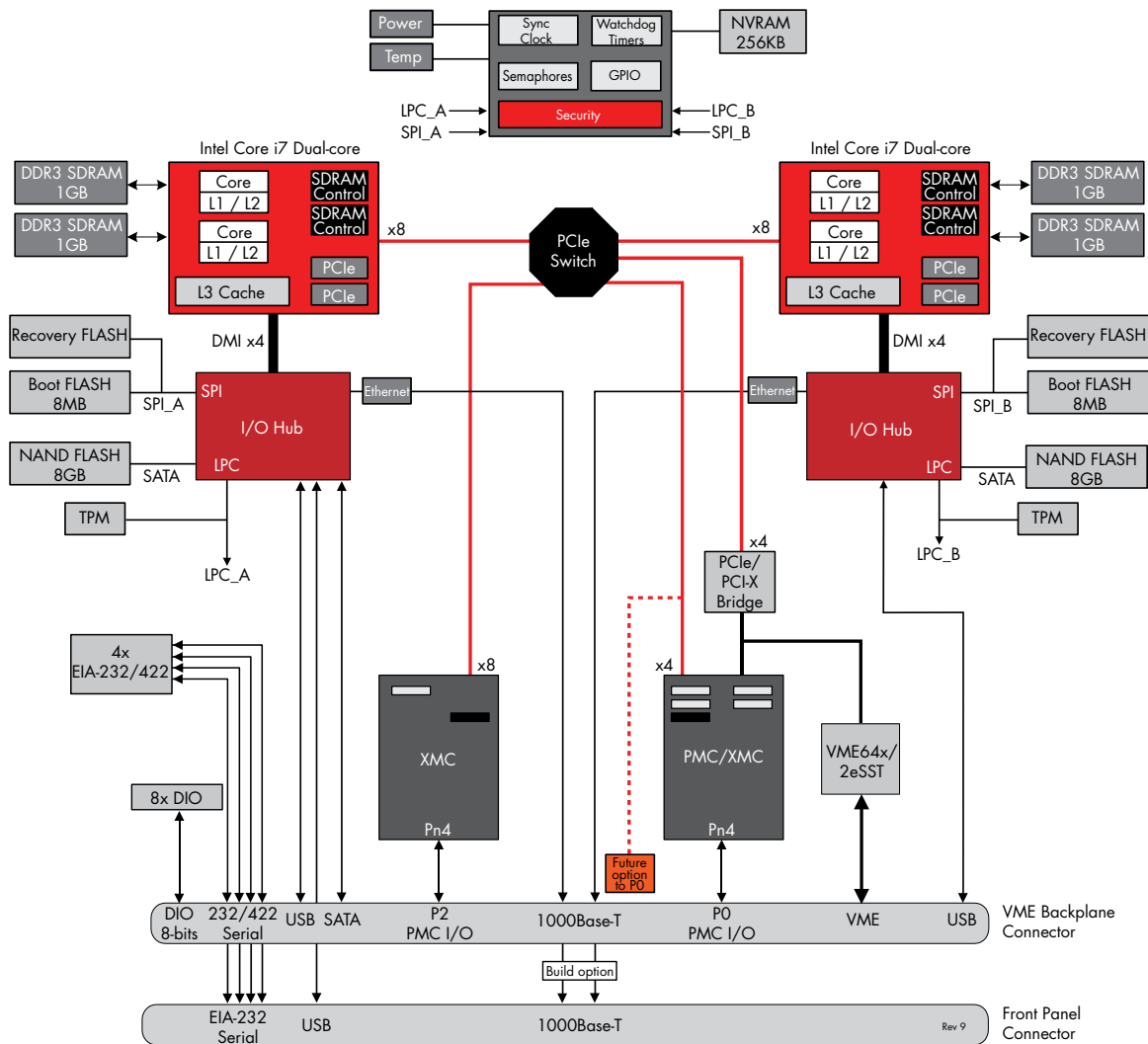
## Warranty

This product has a one year warranty.

## Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

## Technical Support

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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