Data Sheet

CHAMP-AV IV

Quad PowerPC™ MPC7447A/7448 VME Card with QuadFlow Architecture

Features

- Four PowerPC™ MPC7447A/7448 CPUs up to 1.25GHz
  - 64Kbytes L1 and 1Mbyte (MPC7448) L2 internal caches operating at core speed
  - Up to 40 GFLOPS peak computational power
- Up to 512Mbytes DDR-250 SDRAM with ECC per processor
- 256Mbytes FLASH with write protection
- 128Kbytes NVRAM
- QuadFlow architecture with 3.2GB/s peak on-board throughput
- Gigabit Ethernet with on-board switch
  - Each processor has GbE connection to on-board GbE switch
  - Two ports from GbE switch routed to backplane
  - Backwards compatible with 10/100Mbps Ethernet
- VME64x, 2eVME, and 2eSST protocols supported
- Support for two 64-bit, 100MHz PCI-X mezzanine modules
- Four EIA-232 serial ports, one per processor node
- Support for StarFabric PMC modules with differential routing to backplane
- Multi-board synchronous time-stamping feature
- Eight discrete LVTTL I/O signals
- Eight external interrupt inputs
- VxWorks® Board Support Package
- Linux® support from Curtiss-Wright
- Continuum Vector DSP Function Library
- Range of air- and conduction-cooled ruggedization levels available

Overview

The CHAMP-AV IV is Curtiss-Wright Controls Embedded Computing (CWCEC) fourth generation quad PowerPC AltiVec DSP board. The CHAMP-AV IV employs the independent node QuadFlow architecture of the AV II and AV III products, with enhanced performance provided by the latest Freescale Power Architecture™ MPC7447A/7448 PowerPC processors. The CHAMP-AV IV is a component of CWCEC's signal processing system family which includes FGPA processing of the CHAMP-FX, high performance I/O of the StarReach PMC carrier all interconnected with StarFabric switched fabric technology and supported with Inter-Processor Communications software that abstracts the system components to a simple software interface. The CHAMP-AV IV provides the latest in networking technology with Gigabit Ethernet and on-board switching, allowing systems to be networked together with or without external GbE switches.

QuadFlow Architecture

The CHAMP-AV IV architecture is suited to DSP applications that place a high premium on processor to memory, processor to processor, and PMC I/O to memory bandwidth. The data flow capabilities of the CHAMP-AV IV ensure that applications can extract the most from the raw computing performance of the four AltiVec engines. The CHAMP-AV IV architecture encompasses three key attributes that contribute to maximizing DSP performance:

- The performance of the processor, I/O and memory subsystems.
- High-bandwidth, low-latency connections between processor nodes.
- A non-blocking architecture with added data paths for simultaneous data transfers.

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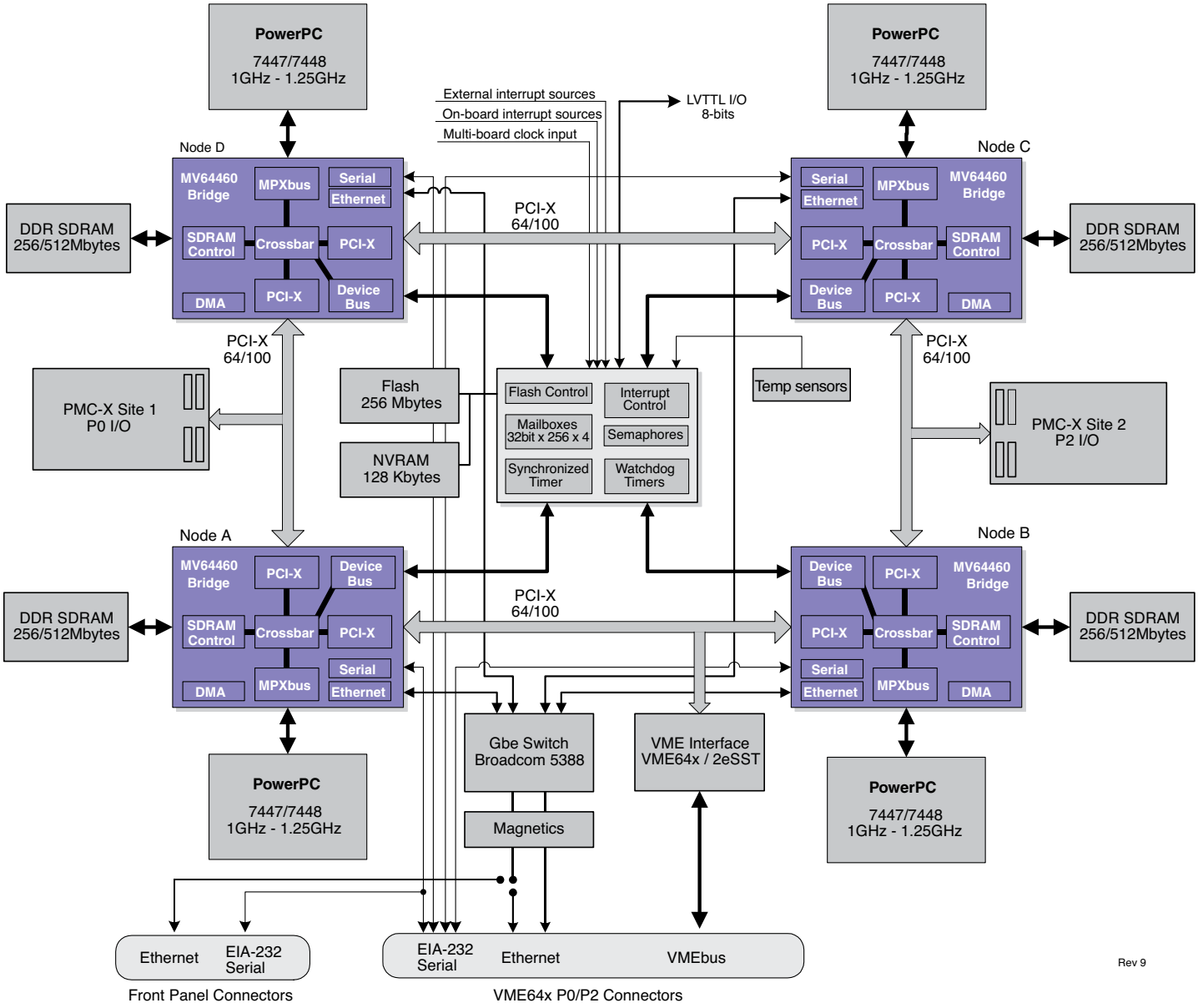
Figure 1: CHAMP-AV IV Block Diagram



Processor Nodes

The CHAMP-AV IV provides four high-performance processing nodes connected in a ring via high speed PCI-X buses. Each node consists of a PowerPC processor and it's own dedicated bank of DDR-250 SDRAM. Each processor node incorporates a Marvell GT64460 Discovery™ III bridge which acts as a non-blocking crossbar interface between the MPC744x, the DDR SDRAM, and two 64-bit, 100MHz PCI-X buses. Each node is provided with a Gigabit Ethernet (GbE) interface.

The Discovery III supports the PowerPC MPX mode of processor bus operation, providing higher memory bus performance compared with the 60x bus. Each node connects to its two adjacent nodes via the pair of PCI-X interfaces. Each node has a separate port into an inter-processor messaging accelerator. With each PowerPC having a dedicated bus to its own memory, applications performance does not degrade as it does in shared memory designs.

In multi-processing applications, problems are either addressed by spreading the data set across many processors or by utilizing the processors in a pipeline, with each processor performing a stage of the algorithm. In either case, the application requires the transfer of data between processors. The data movement is often the limiting feature of board performance rather than raw computing power. The QuadFlow architecture satisfies the processing and data flow requirements of high performance embedded systems.

Each processing node has two independent 64-bit, 100MHz PCI-X connections, one to each of the adjacent nodes. Separate, simultaneous transfers can occur on all four (QuadFlow) of the PCI-X segments, resulting in a peak aggregate bandwidth of 3.2GB/s. The peak PCI bandwidth into any one node is 1.6GB/s.

Each Discovery III bridge provides a four-channel DMA controller which is typically used for managing transfers between processor node memory banks and transfers to and from PMC devices.

The memory map of the CHAMP-AV IV allows any processor to access the memory of any other processor and both PMC sites. Any PMC module or a VME master can access any of the processor node memories.

Double Data Rate SDRAM

Each processor node on the CHAMP-AV IV includes 256 or 512Mbytes of Double Data Rate (DDR) SDRAM. The instantaneous peak data transfer rate to the DDR-250 SDRAM is 2.0GB/s. The memory is protected with Error Checking and Correcting (ECC) circuitry that can detect and correct all single-bit errors and detect all double-bit errors. The DDR SDRAM is accessible from the processor and from both PCI buses and the VMEbus.

FLASH Memory

The CHAMP-AV IV provides 256Mbytes of contiguous, directly accessible, 32-bit FLASH memory on node A. The FLASH interface supports 128MB/sec transfer rates to minimize boot and program loading times.

For absolute security against inadvertent FLASH programming or corruption, a hardware jumper is provided to disable write access to the FLASH.

256Kbytes High Speed SRAM

Incorporated into the Discovery III system controller, the CHAMP-AV IV provides 256Kbytes of high-speed SRAM. While useful as a general purpose high-performance memory area that off loads traffic to SDRAM, the SRAM is particularly beneficial for holding descriptors for Discovery III peripheral devices, allowing DMA units to simultaneously access data from SDRAM while descriptors are accessed from the SRAM.

Gigabit Ethernet With On-board Switching

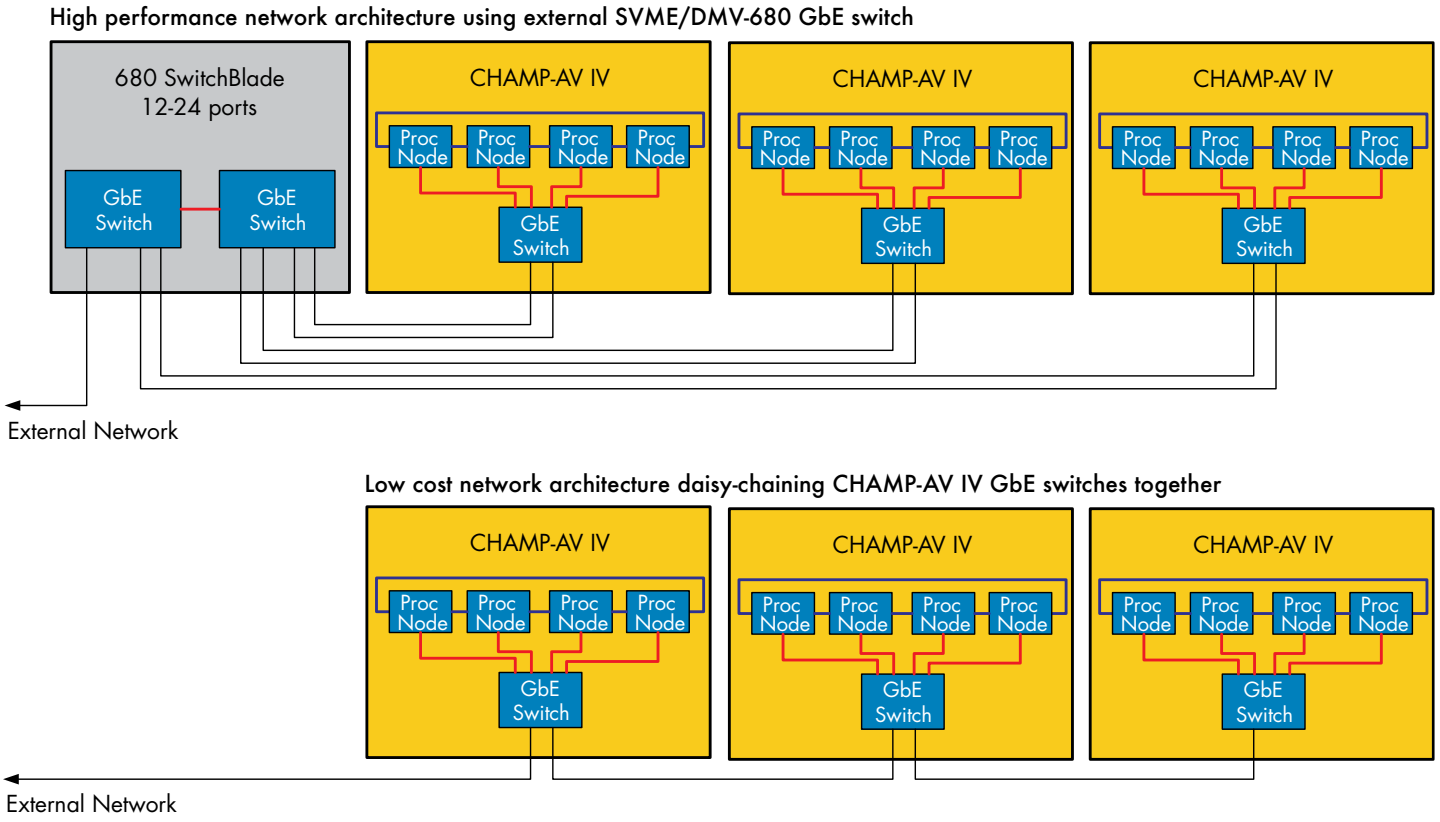
Each processor node of the CHAMP-AV IV is equipped with a GbE interface, implemented via their respective Discovery III bridge. The Discovery III Ethernet controllers integrate a number of features designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for jumbo packets up to 9Kbytes, efficient buffer management schemes, and checksum calculations for IP, TCP and UDP.

The GbE interface of each processor node is routed to an on-board Broadcom 5388 8-port GbE switch. Two ports from the switch are routed to the P2 connector. The on-board switch permits network access to all the processors via either or both of the external GbE ports. The CHAMP-AV IV can be used in high-performance networking environments in conjunction with the CWCEC SVME/DMV-680 SwitchBlade GbE switch, or if the network traffic is less demanding, multiple CHAMP-AV IV cards may be daisy-chained together relying on the on-board switch to route packets to the adjacent card as needed. See Figure 2 for example networking architectures.

PMC-X Sites

The CHAMP-AV IV is equipped with two mezzanine sites capable of PCI (PMC) or PCI-X (PMC-X). The PMC-X interfaces support 64-bit, 100MHz PCI-X transfers with a resulting peak rate of 800MB/s. The board is backward compatible with either 32-bit or 64-bit PMCs at 33 or 66MHz. The PMC-X interfaces are mapped to all four processor nodes allowing transfers between any node and any PMC-X interface. All four PMC interrupt signals may be routed under software control to any of the processors, allowing the developer the choice of which processor hosts PMC control software.

Figure 2: Example Networking Architectures



The conduction-cooled versions of the CHAMP-AV IV adhere to the IEEE 1386-2001 and ANSI/VITA 20 standard for conduction-cooled PMCs. The CHAMP-AV IV thermal frame provides the best possible thermal interface for PMC modules by supporting the primary and secondary thermal interfaces as defined by ANSI/VITA-20. To support high performance PMCs such as our PMC-704 graphics module and the PMC-643 Fibre Channel module, the CHAMP-AV IV thermal frame supports a mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed PMC modules can significantly lower the temperature rise between the CHAMP-AV IV card edge and the PMC components. The mid-plane thermal shunt does not impinge on the IEEE 1386-2001 specified component height.

PMC I/O is supported on both the front panel (air-cooled) as well as the P2/P0 backplane connectors. The routing of I/O signals from PMC to P0 and P2 is arranged in differential pairs with careful impedance control and matching of trace lengths. This technique supports the latest generation of high performance digital interfaces included on some PMCs, such as our StarLink-II switch fabric PMC and PMC-643 Fibre Channel. With a pair of StarLink-II PMCs, the CHAMP-AV IV can act as a combined StarFabric node and switch, with a massive 3.2GB/s of I/O (including switching throughput) between the PMCs and the I/O connectors. The mapping between PMC site 2 and the P2 connector is in accordance with draft standard VITA-35. The mapping between PMC site 1 and the P0 connector follows the proposed draft standard VITA-31, with an additional 16 signals.

Inter-processor Messaging Accelerator

In multi-processing applications, software designers implement message passing schemes between the various processors in the system. The most common implementation is for the transmitting processor to cause an interrupt to occur on the receiving processor, with a pre-agreed protocol between the pair to define the location and content of the message.

The problem with this mechanism is that many board architectures suffer latencies and other slowdowns because the same PCI bus that is used for inter-processor data transfers is also used for passing these interrupts. The CHAMP-AV IV has special purpose hardware to accelerate inter-processor messaging. Each node has a separate non-PCI interface into this messaging accelerator. See Figure 2: Processor Node Block Diagram for details. The accelerator provides three key functions to speed the delivery of messages between processors.

- Processor to Processor Mailbox Interrupts
- Hardware Interrupt Routing
- Semaphores

The accelerator provides mailbox interrupts, whereby a processor can interrupt another processor and deliver a 32-bit value. Each processor has a 32-bit, 256-deep FIFO. Any processor can write to the FIFO of any other processor. An entry in the FIFO causes an interrupt to the associated processor, if enabled. The software can use the 32-bit value to include a message with the interrupt. The combination of a separate data path and the inclusion of a 32-bit message can significantly reduce the latency of using interrupts to send messages between processors.

The accelerator also provides an interrupt routing function. In a single processor system, it is obvious where all interrupt processing tasks are handled. In a quad processor system, a fixed mapping of hardware interrupts to specific processors is likely to be less then optimum. The CHAMP-AV IV allows the hardware to adapt to the needs of the software.
All of the internal and external interrupt sources (PMC modules, VME, GPIO, PCI, etc.) are routed into a software configurable multiplexer that allows any processor to receive interrupts from any device. This feature speeds interrupt response time by routing the interrupt directly to the intended processor. Since the interrupt status registers are within the accelerator, the application avoids using the PCI bus during the interrupt service routine, thus reducing the incurred latency.

The accelerator provides sixteen hardware semaphore registers which are typically used to coordinate the sharing of hardware resources between multiple tasks. The hardware solution provides a faster alternative to traditional software/memory techniques and avoids the use of shared memory and PCI buses to access the semaphores.

VMEbus Interface

The CHAMP-AV IV is equipped with a VME master/slave interface that supports the VME64x, 2eVME, and 2eSST protocols. The interface is implemented with the Tundra Tsi148 PCI/X to VME bridge. The Tsi148 supports the newest 2eSST VMEBus transfer protocol offering the maximum possible VME performance, while retaining full backwards compatibility with legacy VME systems. All the processor nodes of the CHAMP-AV IV can be mapped to have direct access to the VMEbus, or use the Tsi148 internal DMA engines to move data between local memory and the VMEbus.

Serial Ports

The CHAMP-AV IV provides four EIA-232 serial ports, one connected to each processor node. The serial ports are implemented with the Discovery III Multi-Protocol Serial Controllers. The serial ports each provide a transmit and receive signal which are routed to the CHAMP-AV IV backplane connectors.

General Purpose I/O and Interrupt Inputs

The CHAMP-AV IV provides eight general purpose LVTTL I/O lines which are accessible at the P2 connector. The GPIO signals may be configured individually to be inputs or outputs. Outputs may be configured to be open drain or LVTTL. Each signal is pulled up to 3.3V through a 10 KΩ pull-up resistor. Note that 3.3V LVTTL is interoperable with 5V TTL logic.

Eight of the GPIO lines may be configured to act as edge or level sensitive interrupt inputs. This flexibility can save a user from building custom logic to condition signals to be used as interrupt sources. Also, one of the GPIO pins may be optionally used for the multi-board synchronization functionality.

Indicator LEDs

The CHAMP-AV IV provides twelve user-controllable LEDs. Four of these are visible on the front panel of the air-cooled version, and eight more are located on the back of the board. For both air- and conduction-cooled cards, there is an additional red LED on the front panel used to indicate a failure determined by the on-board diagnostic firmware.

Timers

The CHAMP-AV IV board provides a large number of timing resources to facilitate precise timing and control of system events. A list of available timers is given in the table below.

Table 1: Specifications

Timer Facility	Implementation	Type	Size	Tick Rate/ Period	Maximum Duration
PowerPC	CPU	Free running counter	64-bit	31.25Mhz/32ns	18,718 years
Time Base Register					
PowerPC	CPU	Presettable, readable downcounter	32-bit	31.25Mhz/32ns	137.4 sec.
Decrementers					
General Purpose #0-3	Discovery III	Presettable, readable downcounter with autoreload or stop options	32-bit	125.0Mhz/8ns	34.3 sec.
Watchdog Timers (one per CPU)	Core Functions FPGA	Presettable, readable downcounter with interrupt or reset on terminal count	24-bit	1Mhz/1µs	16.7 sec.
Multi-board Synchronous Timer	FPGA	Presettable, readable	48-bit	16MHz/62.5ns	203.6 days

Multi-board Synchronous Timebase

The CHAMP-AV IV includes a special purpose counter which can be synchronized with corresponding counters on other boards in the same VME system. This common timebase allows a developer to time-stamp messages and/or data buffers, with the knowledge that the local time is maintained at the same value by all the boards in the system. This feature is typically most valuable for debugging and instrumenting multi-board applications code, which can present challenges in coordinating the distribution of data items between processors.

Avionics Style Watchdog Timer

The CHAMP-AV IV provides four watchdog timers, one for each processor. Each watchdog timer is a presettable down counter with a resolution of 1ms. Time-out periods from 1ms to 16 seconds can be programmed. Initialization software can select whether a watchdog exception event causes an interrupt or a card reset. Once enabled to cause a reset, the watchdog cannot be disabled.

The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in "Avionics" mode whereby a minimum interval between writes to the watchdog register is also enforced. In other words, writing to the watchdog register too soon or too late causes an exception event.

Temperature Sensors

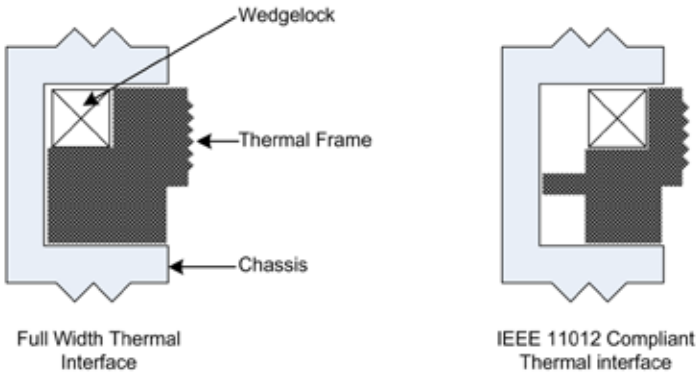
The CHAMP-AV IV provides temperature sensors to measure board and processor temperatures. Software can read the temperature sensors at any time through the Discovery III I2C interface. The temperature sensors have user-configurable threshold detection registers and are accurate to +/- 2.5°C.

Full-Width Thermal Interface

Conduction-cooled versions of the CHAMP-AV IV employ a thermal frame design which reduces thermal contact resistance to the chassis. As illustrated in Figure 3, this is accomplished by extending the frame to the full width of the card. This is a small deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in standard air-cooled chassis. The reduced temperature rise across the card to chassis contact, allows for the chassis to operate several degrees hotter while still maintaining the specified card edge temperature.

For cooling concerns it is not recommended to operate a conduction-cooled CHAMP-AV IV in an air-cooled enclosure. However, with proper attention to cooling and monitoring of temperatures, it is possible to remove the card guides from most air-cooled enclosures to accommodate installation of the board.

Figure 3: Full width thermal interface



Built In Test Firmware

The CHAMP-AV IV is provided with a firmware package that performs board initialization and Built In Test (BIT). The BIT routines support Power-up BIT (PBIT) and Initiated BIT (IBIT).

The PBIT consists of a set of essential tests that provide confidence that the hardware is operating correctly while minimizing power-up time. The IBIT capability allows users to initiate testing with a more comprehensive suite of tests to provide more robust testing in an off-line mode. The selection of tests for PBIT and IBIT is configurable.

Operating System Software

The CHAMP-AV IV is supported with an extensive array of software items, which cover all facets of developing application code for the board. Users have the option of choosing to develop with a variety of operating systems and development tools. The following operating systems are supported on the CHAMP-AV IV:

- A VxWorks® (Tornado™) from Wind River®. (Part number DSW-416-000-CD. See separate CHAMPTools datasheet for details.)
- Linux Software Development Suite. (Part number DSW-416-6100-ELDK)

Optimized DSP Libraries

The CHAMP-AV IV derives its floating-point performance from the PowerPC AltiVec unit. Programming the AltiVec is complex. For customers who prefer to focus on their algorithms, CWCEC offers the Continuum Vector DSP function library. Vector provides over 200 functions, providing the foundation for most signal processing applications. Continuum Vector provides the user with a choice of APIs with support for Vector Signal Image Processing Library (VSIPL, Core Lite) standard and the popular API established by Floating Point Systems Inc. See the Continuum Vector datasheet for detailed information.

Inter-Processor Communication Library

The Inter-Processor Communication Library (IPC) is a library of functions designed to enable high performance, low latency message passing. IPC allows processors to communicate task-to-task on the same card or within the StarFabric network. It also provides low-overhead block data transfers, segmented block data transfers and signaling between processors to assist in high bandwidth data movement. See the IPC Library datasheet for more details.

Designed for Harsh Environments

To cost-effectively address a diverse range of military/aerospace applications, the CHAMP-AV IV is available in a range of ruggedization levels, both air- and conduction-cooled. All versions are functionally identical, with air-cooled versions (SVME) and conduction-cooled (DMV) in levels 100 and 200. Our standard ruggedization guidelines define the environmental tolerance of each ruggedization level. See the Ruggedization Guidelines datasheet for more information.

To ensure a long in-service life for the product, we carefully analyze the projected fatigue life of solder joints and interconnections. The mounting of all components is reviewed to ensure that differential thermal expansion between the component and the Printed Wiring Board (PWB) does not unduly shorten the fatigue life of the solder joints.

Ordering Information

The CHAMP-AV IV is ordered with the following part numbers. SVME-416-xyyy denotes air-cooled versions of the product, where "x" defines the ruggedization level, (0,1,2 etc.) and "yyy" identifies a specific configuration. DMV-416-xyyy denotes conduction-cooled versions of the product, following the same conventions. Note that a configuration may also include one or more installed PMC modules. A formal quote from CWCEC or authorized representative will provide a complete part number and description of the configuration.

Specifications

The CHAMP-AV IV is available in a full range of environmental grades starting from commercial air-cooled to extended temperature, rugged conduction-cooled versions. This allows the customer to select the board to match the environmental requirements of the platform.

Table 2: Power, dimensions and weight characteristics

Power Requirements (without PMCs)		
5.0V	12A - 15A typical (7448)	
3.3V	1A typical (7448)	
12.0V	Only used for PMC power	
-12.0V	Only used for PMC power	
Dimensions and Weight		
Option	Dimension	1250g (2.75lbs)
Air-cooled	Per ANSI/VITA 1-1994	<570 grams (1.26lbs)
Conduction-cooled	Per IEEE 1101.2-1992	<750 grams (1.65lbs.)

Note: Air-cooled cards available in level 0 and level 100.*
Note: Conduction cooled cards available in level 100 and level 200.*
*Refer to Ruggedization Guidelines data sheet for more information.

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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