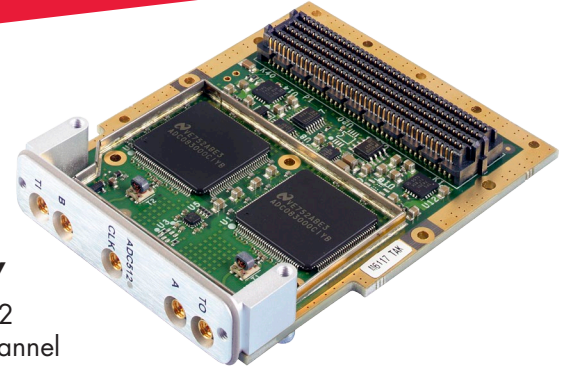




ADC512

Dual Channel 3 GSPS 8-bit
Analog Input FMC



Applications

- ◆ Signal Intelligence (SigInt)
- ◆ Electronic Counter Measures (ECM)
- ◆ Radar

Features

- ◆ Dual 3 GSPS 8-bit ADCs
- ◆ 2.6 GHz input bandwidth
- ◆ FMC/VITA 57 form factor
- ◆ Air- or conduction-cooled rugged versions

Benefits

- ◆ Direct ADC connection to host FPGA ensures maximum throughput
- ◆ Able to synchronize multiple channels/boards
- ◆ Easily interfaces to FPGA-based host board
- ◆ Complete ADC I/O

Overview

The ADC512 is a dual channel 3 GSPS analog input FPGA Mezzanine Card (FMC) based on the VITA 57 specification. This specification allows I/O devices to be directly coupled to a host FPGA. On the ADC512, the two ADC devices connect through the high bandwidth FMC connector to an FPGA-based host board which maximizes data throughput and minimizes latency.

The ADC512 supports an external sample clock input, accepting an input level between -5dBm and +5dBm. The clock signal may be sinusoidal or square. Multiple ADC512 boards can be synchronized to increase the number of input channels. The ADC512 can be used on platforms like Curtiss-Wright's FPE320, FPE650, HPE720 and VPX6-472.

Analog Input

The ADC512 supports two analog inputs through 50Ω MMCX type front panel connectors. The analog inputs are single ended and are coupled to the ADCs using a balun and AC coupling capacitor configuration to produce the broadband differential input required by the devices. The analog signal paths of both ADC inputs are matched to within 1 ps to allow synchronous operation of the ADCs. The "Full Scale" analog input voltage is 700mVpp at 10 MHz but may be varied between 560 and 840mVpp by setting ADC registers. Maximum input is +/- 3VDC, 2Vpp AC(+ 10dBm).

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Clock, Trigger & Synchronization

The external front panel clock input is through a 50 Ω MMCX type front panel connector. The clock input is designed to operate at a typical frequency of 1.5 GHz but may operate at clock frequencies of down to 500 MHz and up to 1.5 GHz. The clock input is designed to operate with an input level between -5 dBm and +5 dBm. The clock input may be sinusoidal or square. The analog sampling clock is derived from clocking on both the rising and the falling edge of the 1.5GHz input clock.

Trigger In and Trigger Out use 50 Ω MMCX type front panel connectors. Actual functionality of these signals is dependent on the HDL code in the FPGA of the host carrier card.

Trigger In is a single ended LVPECL input signal. The maximum operating frequency of this input is designed to be approximately 300 MHz.

Trigger Out is a single ended LVPECL output signal.

It is possible to synchronize the ADCs on multiple ADC512's using the Trigger In & Trigger Out signals. The ADC512 FusionXF HDK & SDK support this functionality.

FusionXF Software/HDL Support

Curtiss-Wright's FusionXF development kit includes software, HDL and utilities with examples and infrastructure for using the ADC510 on each supported host.

One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA. It facilitates the inclusion of signal processing blocks such as digital down converters, making HDL development easier and integration more straightforward.



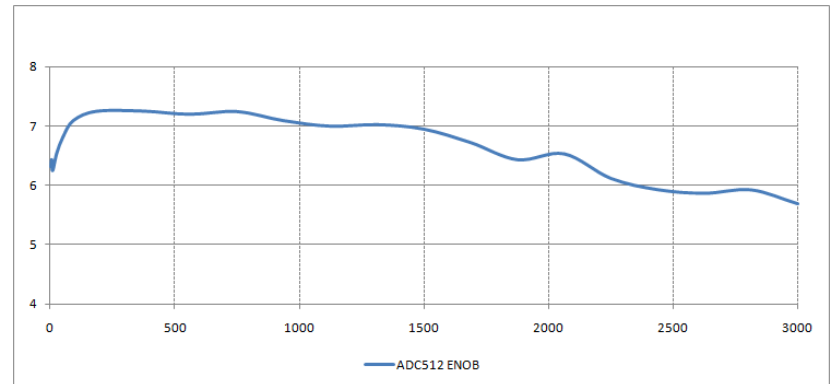
Analog Performance

The following figures provide data from Curtiss-Wright's preliminary analog characterization of the ADC512. They represent typical measured performance.

Effective Number of Bits (ENOB)

The ADC512 shows an ENOB greater than 7-bits for the majority of the 1st and 2nd Nyquist zones. Performance correlates favorably, within 0.2-bits, to the National Semiconductor datasheet for frequencies up to 1500 MHz.

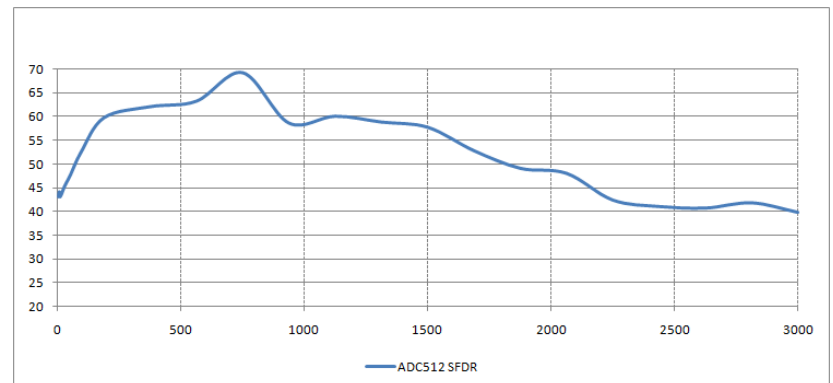
Figure 1: ADC512 ENOB



Spurious Free Dynamic Range (SFDR)

The SFDR is shown below. The main non-linear element in the ADC512 is the balun which performs the broadband single-ended to differential signal conversion required for input to the ADC chip.

Figure 2: ADC512 SFDR



Signal to Noise Ratio (SNR)

The ADC512 board exhibits similar characteristics to the ADC083000 analog to digital converter.

Figure 3: ADC512 SNR

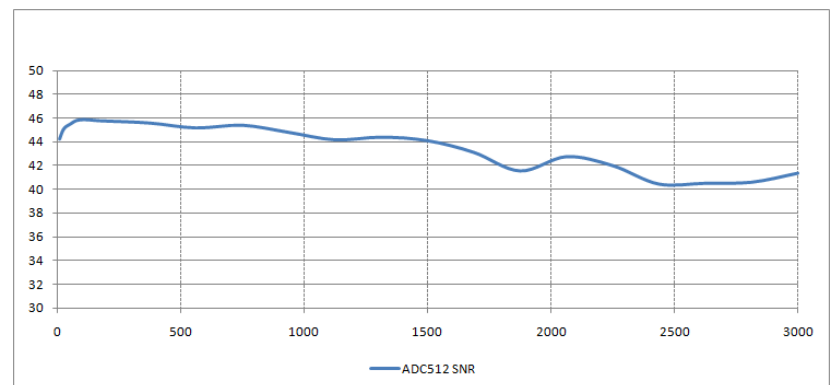




Table 1: Ordering Information

Part Number	Number of channels	Coupling	On-board Clock	RoHS Compliant or Lead Solder Process	Ruggedization Level	Air-Cooled	Rugged Air-Cooled	Conduction-Cooled	Conformal Coating
ADC512-02	2	A/C: Balun	-	RoHS	AC 0	✓	-	-	-
ADC512-02-B1H	2	A/C: Balun	-	RoHS	AC 100	-	✓	-	✓
ADC512-02-D5H	2	A/C: Balun	-	RoHS	CC 200*	-	-	✓	✓
ADC512-02L	2	A/C: Balun	-	Lead Solder Process	AC 0	✓	-	-	-
ADC512-02L-B1H	2	A/C: Balun	-	Lead Solder Process	AC 00	-	✓	-	✓
ADC512-02L-D5H	2	A/C: Balun	-	Lead Solder Process	CC 200*	-	-	✓	✓

*Contact factory

Table 2: Specifications

Analog Input	
Number of Channels	2
Sampling Frequency	Up to 3 GSPS
Full Scale Input Voltage	600 - 820mVpp (adjustable via register settings)
Device	2x National Semi ADC083000
Input Bandwidth (3dB)	2.6 GHz
Input Impedance	50 Ohm, AC coupled
Input Connector	Front panel MMCX
SNR (ADC device)	46.98 dB ¹
SFDR (ADC device)	61.6 dBc ¹
ENOB (ADC device)	7.45 bits ¹
Clock & Trigger Inputs	
Clock Input Connector	Front panel MMCX
Clock Input	50 Ohm, AC coupled LVPECL
Clock Input Frequency	500 MHz to 1.5 GHz. Sampling is on both rising & falling clock edges (i.e. 1.5 GHz clock = 3 GSPS)
Trigger Input/Output	Single-ended, 50 Ohm, LVPECL buffered to host FPGA

Software/HDL	
Host HDL Code	Analog input hosted by FusionXF on FPE650 6U quad FPGA VPX (contact Curtiss-Wright for other hosts)
Misc.	
LEDs	1x yellow (host FPGA controlled)
I2C bus	Atmel AT24C512B Serial EEPROM; MAX6656 to monitor ADC temp
Environmental	
Ruggedization Levels	Air-cooled Air-cooled Rugged Conduction-cooled

Notes

1. $F_{in} = 748$ MHz; $V_{in} = \text{Full Scale} - 0.5$ dB; $F_s = 1500$ MSPS All the analog characterizations in this datasheet represent the measured performance of a standard production board in normal laboratory conditions. These are typical performance figures and are not guaranteed.



Table 3: Specifications

Part number extension		Air-cooled			Conduction-cooled	
		Level 0	Level 100	Level 200 (Note 6)	Level 100	Level 200
Temperature	Operational (Air-Cooled Note 4) (Conduction-Cooled Note 7)	0°C to +50°C	-40°C to +71°C	-40°C to +85°C	-40°C to +71°C	-40°C to +85°C
	Non-operational (storage)	-40°C to +85°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C	-55°C to +125°C
Vibration	Sine (Note 1)	2g peak 15-2k Hz	10g peak 15-2k Hz	10g peak 15-2k Hz	10g peak 15-2k Hz	10g peak 15-2k Hz
	Random (Note 2)	0.01g2/Hz 15-2k Hz	0.04g2/Hz 15-2k Hz	0.04g2/Hz 15-2k Hz	0.1g2/Hz 15-2k Hz	0.1g2/Hz 15-2k Hz
Shock (Note 3)	Operational	20g peak	30g peak	30g peak	40g peak	40g peak
Humidity	Operational	0-95% non-condensing	0-100% non-condensing	0-100% non-condensing	0-100% non-condensing	0-100% non-condensing
	Non-operational (storage)	0-95% non-condensing	0-100% condensing	0-100% condensing	0-100% condensing	0-100% condensing
Conformal Coat (Note 5)		No	Yes	Yes	Yes	Yes
2 Level Maintenance Ready		-	-	-	No	No

Notes:

1. Sine vibration based on a sine sweep duration of 10 minutes per axis in each of three mutually perpendicular axes. May be displacement limited from 15- 44Hz, depending on specific test equipment.
2. Random vibration 60 minutes per axis, in each of three mutually perpendicular axes.
3. Three hits in each axis, both directions, 1/2 sine and saw tooth. Total 36 hits.
4. Standard air-flow is 8 cfm at sea level. Some higher-powered products may require additional airflow. Consult the factory for details.
5. Conformal coating type is manufacturing site specific. Consult the factory for details.
6. This is a non-standard product. Consult factory for availability.
7. Temperature is measured at the card edge.

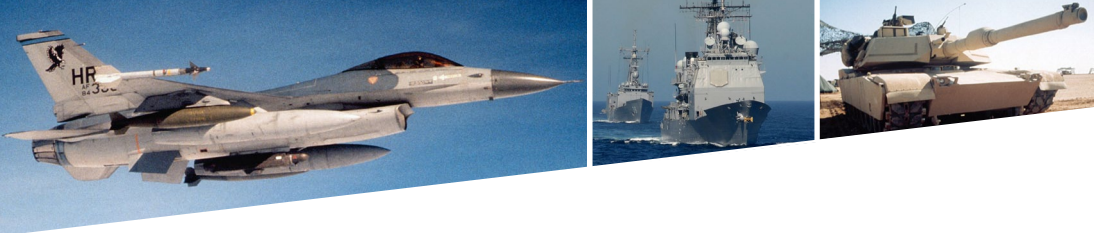
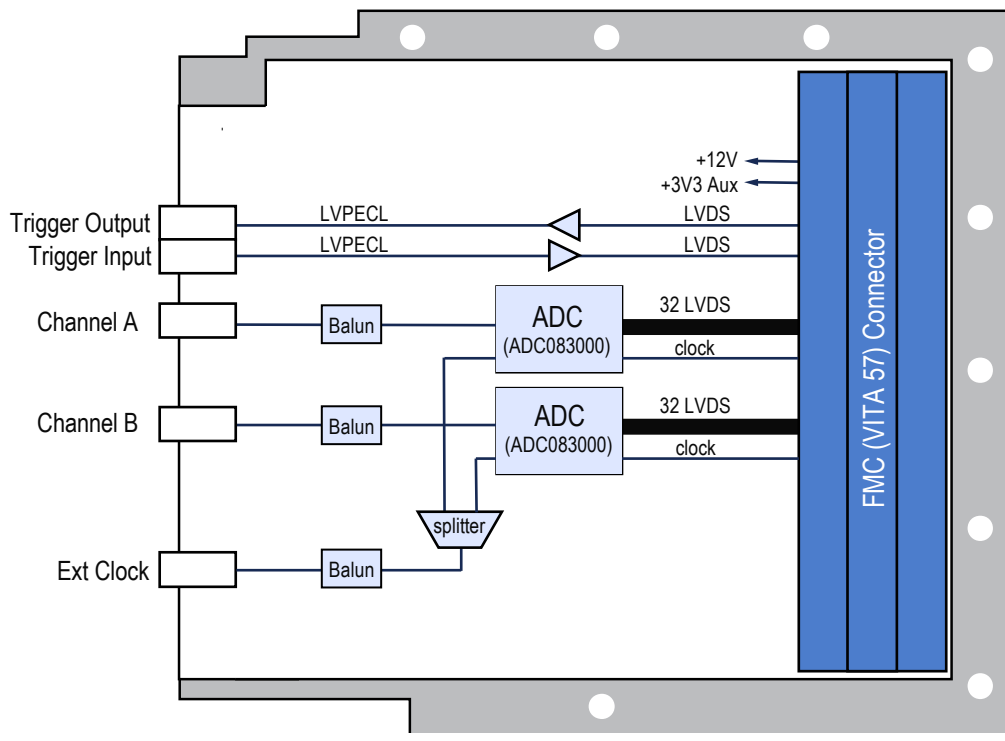


Figure 4: ADC512 Block Diagram



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:
 Website: www.cwembedded.com/sales
 Email: sales@cwembedded.com

Technical Support

For technical support:
 Website: www.cwembedded.com/support
 Email: support1@cwembedded.com

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