



# AD3000

## 3GSPS Analog Input XMC/PMC with Xilinx® Virtex®-5 FPGA



### Applications

- ◆ Electronic Warfare (EW)
- ◆ Spectral Analysis
- ◆ RADAR

### Features

- ◆ 3GSPS, 8-bit ADC
- ◆ Xilinx Virtex-5 SX95T FPGA (user programmable)
- ◆ Dual banks of QDR SRAM and DDR SDRAM memories
- ◆ Capable of multi-board synchronization
- ◆ XMC/PMC form factor (including rugged)
- ◆ Windows®, VxWorks® and Linux® support

### Benefits

- ◆ Combined acquisition and data processing
- ◆ Lower power solution
- ◆ Suitable for use in severe environments
- ◆ Industry standard form factor
- ◆ PCI Express® provides high throughput to baseboard

### Overview

The AD3000 closely couples a high performance Xilinx Virtex-5 FPGA to a high-speed analog input front end providing both processing and up to 3GSPS acquisition in a single XMC/PMC card. The combination of a user programmable FPGA, data I/O sub-systems and multiple banks of fast memory provides a powerful platform for acquiring and processing high-speed data in one board. In addition to processing digitized data, the Xilinx Virtex-5 SXT FPGA is used to control the analog to digital converter and provides the off-board interfaces to either PCI-X or the multi-GB/s serial I/O used for the XMC interface.

### Analog I/O & FPGA Processing in One

The AD3000 is a combined acquisition and FPGA based data processing module. The majority of the Virtex-5 FPGA resources are available for user programmable processing and are supported by SRAM and SDRAM memories. Some applications that are ideally suited for FPGA based processing include Digital Down Conversion (DDC), Fast Fourier Transforms (FFTs) and digital filters.

### 3GSPS Analog Input

Analog to digital conversion is performed by a National Semiconductor ADC083000 device, which is an 8-bit, 3GSPS ADC. The analog input stage is transformer AC coupled to the ADC via a balun. The full power input bandwidth of the AD3000 is 2.25GHz (3dB), though input frequencies up to 3GHz can also be sampled. Using the ADC's built-in demultiplexer, digitized data is transferred to the FPGA using a 32-bit interface (4 samples in parallel) at one 8th of the sampling rate along with a quarter of clock frequency (double edge clocking) to match valid data.

Learn More

Web / [sales.cwembedded.com](http://sales.cwembedded.com)

Email / [sales@cwembedded.com](mailto:sales@cwembedded.com)

**ABOVE & BEYOND**

**CURTISS  
WRIGHT** Controls  
Embedded Computing  
[cwembedded.com](http://cwembedded.com)



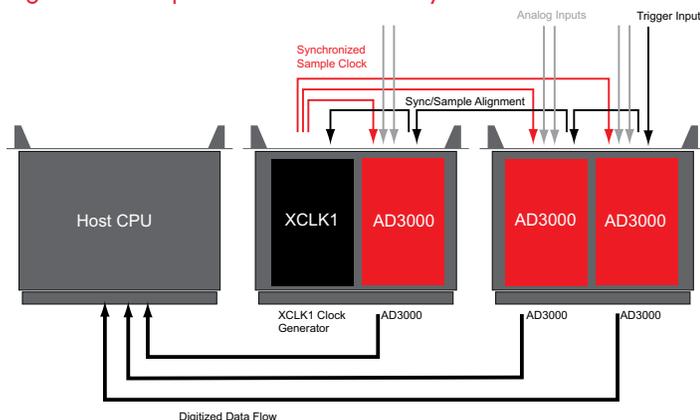
## Clocks, Triggers & Multi-board Synchronization

The AD3000 provides a front-panel MMCX connector for connecting an external sample clock source (required). The input clock rate to the AD3000 is 1/2 of the ADC sample rate as the ADC device uses double edge clocking (i.e. a 1.2GHz clock source is required to digitize data at 2.4GSPS).

A front panel mounted trigger input (TI) and a trigger output (TO) signal are connected to the FPGA via LVPECL I/O stages. This allows the FPGA to define the trigger mechanism through the application for maximum flexibility.

The AD3000 supports multi-board synchronization allowing all ADCs to be synchronized to a common clock source. When synchronized, all data will be aligned and coherent across multiple AD3000 boards. Curtiss-Wright's XCLK1 clock generator is capable of providing this synchronized sample clock output to two or more AD3000 ADCs, providing support for features such as synchronous reset of the sample clock.

Figure 1: Multiple AD3000s can be synchronized



## Xilinx Virtex-5 FPGA

The AD3000 is fitted with a Xilinx Virtex-5 SX95T FPGA (contact Curtiss-Wright for availability of other FPGA variants) which is optimized for a high ratio of DSP blocks to standard logic blocks to support high performance signal processing.

The FPGA is configured at power up from FLASH with a default image, a recovery image or an image the customer generates. In addition to FLASH configuration, new images can be downloaded from the host via the PCI or PCI Express (PCIe) interface. Software is provided to load new images into either FLASH or SRAM. Bit streams stored in SRAM benefit from faster downloads while bypassing non-volatile storage - useful for secure applications.

## Multiple SDRAM & SRAM Banks

The AD3000 features both external SRAM and SDRAM connected to the FPGA. These can be used for buffering ADC data or for general purpose processing support.

The two 128MB DDR2 SDRAM banks on the AD3000 can be used in parallel to buffer digitized data. Each bank is 16-bits wide

QDR2 SRAM provides higher bandwidth external memory. Two 2M x 36-bit banks are fitted on the AD3000

## PCI/PCI-X, PCIe & Multi-GB/s I/O

The AD3000 includes a PCI/PCI-X interface, supporting up to 133MHz operation, and a PCIe interface. These interfaces provide multi-channel DMA support.

The PCIe interface uses the Virtex-5 FPGA's RocketIO™ GTP transceivers and an embedded end-point controller. The Virtex-5 FPGA provides sixteen, full duplex high-speed serial communication links through RocketIO GTP transceivers. These links are evenly split between two XMC (VITA 42) connectors. Each link is able to operate at up to 3.2GB/s (using an SX95T FPGA) and can be driven as independent data streams or bonded to create 'fat pipes' for fewer, but higher bandwidth, data streams. A built-in PCIe end-point block allows x4 or x8 lane communications at 2.5GB/s. This is a hard IP block within the Virtex-5 FPGA, which can be bypassed for other protocols such as sFPDP.



## Rugged Build Options

A range of environmental requirements are addressed by the AD3000: air-cooled benign, air-cooled extended temperature, air-cooled rugged and conduction-cooled. For conduction-cooled applications, the host board must be able to incorporate front panel I/O connections. Depending on the application, a suitable heatsink may be required for conduction-cooled builds.

## FusionXF Development Kit

Curtiss-Wright's FusionXF development kit provides examples and infrastructure for using the AD3000 or the AD3000 on one of Curtiss-Wright's other Xilinx Virtex-5 and Virtex-4 FPGA-based products. This includes a C-API and sophisticated DMA support.

One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA. With support for high-speed DMA capabilities and documented interfaces for the integration of custom IP, FusionXF makes HDL development and integration easier.

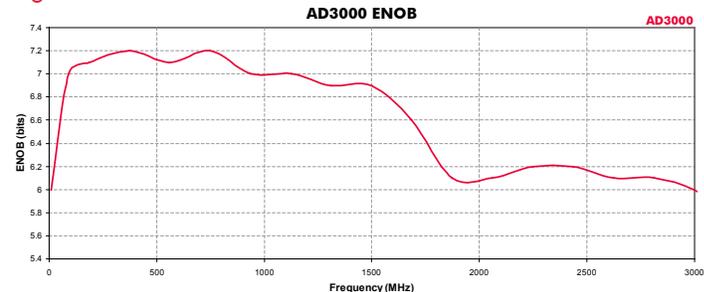
Example software/HDL illustrates how to interface to on-board devices such as QDR SRAM and DDR SDRAM. Under software running on the host, data can be moved to and from the AD3000's memories using FusionXF's high performance DMA capabilities.

Software utilities are provided for configuring the FPGA. These include FLASH programming and commands to configure the FPGA from a given image in FLASH or SRAM. The FPGA may also be configured via a ChipScope™ Pro/JTAG interface. Host operating systems supported include Windows, VxWorks and Linux.

Although the AD3000 is aimed at applications requiring both high-speed digitization and user programmable FPGA processing, a full acquisition-only example image is provided. This allows the AD3000 to be used 'out-of-the-box' without having to develop FPGA code. This image can be loaded from the FLASH file system and supports full bandwidth data acquisition, external trigger modes and high-speed DMA driven PCI-X/PCIe channels to the host processor. This example can be modified to include a user application, making the AD3000 quick and easy to use.

## Analog Performance

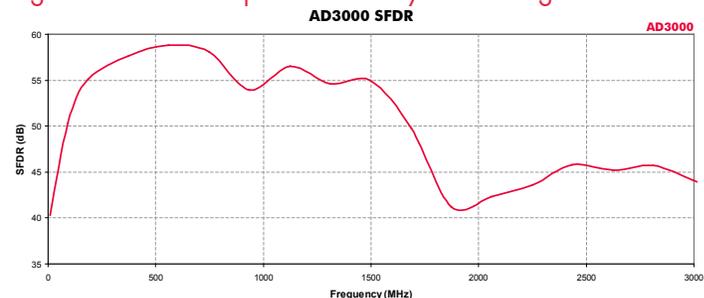
Figure 2: AD3000 Effective Number of Bits



### Effective Number of Bits (ENOB)

The AD3000 exhibits an ENOB greater than or equal to 6-bits for the entire 1<sup>st</sup> and 2<sup>nd</sup> Nyquist zones. This drops below 8MHz. The balun (necessary for wide input bandwidth) at the front end is the primary cause of the low frequency distortion. The AD3000 performance correlates favorably, within 0.5-bits, to the National Semiconductor ADC083000 datasheet for frequencies up to ~2200MHz; the highest frequency for which figures are available as the device ENOB has dropped below 6-bits. The AD3000 shows an improved ENOB over the ADC083000 datasheet at frequencies greater than 2.2GHz.

Figure 3: AD3000 Spurious Free Dynamic Range

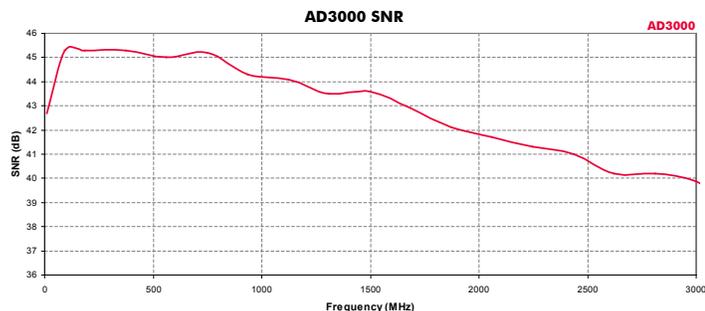


### Spurious Free Dynamic Range (SFDR)

The SFDR is generally dominated by the 2<sup>nd</sup> or 3<sup>rd</sup> harmonics of the input signal which are typically introduced by non-linearities in the system. The main non-linear element of the AD3000 is the balun which performs the broadband single-ended to differential conversion required for the input to the ADC chip. The highest spurious signal is sometimes located at  $(F_{\text{Samp}}/2) \pm F_{\text{Input}}$ , this spurious frequency is caused by the internal folding interpolating architecture of the ADC083000 device.



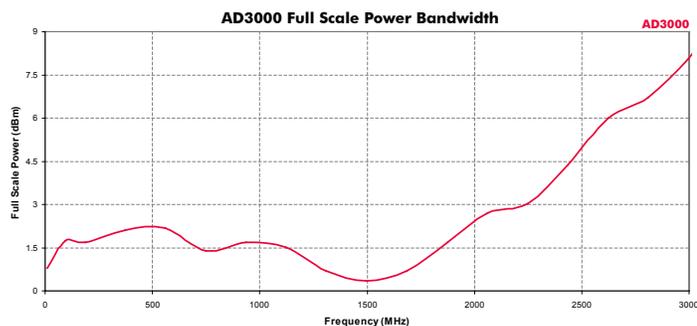
Figure 4: AD3000 Signal to Noise Ratio



### Signal to Noise Ratio (SNR)

The AD3000 SNR compares well with National Semiconductor datasheet at around only 2 dB worse in the 1<sup>st</sup> Nyquist zone, but generally better than or equal to the device datasheet in the 2<sup>nd</sup> Nyquist zone.

Figure 5: AD3000 Full Scale Power Bandwidth



### Gain Bandwidth

The output is normalized to show the input signal level required to give a full scale sampled signal. The AD3000 is shown operating in "Extended Control" mode with the 'Full Scale Voltage Adjust' Register set to 700mVp-p (0.88 dBm). The output shows a 3dB bandwidth of approximately 2200MHz, ie full 1<sup>st</sup> Nyquist and extending to half of the 2<sup>nd</sup> Nyquist zone, with approximately  $\pm 1$  dB Gain Flatness in first Nyquist.

### Sample FFT Plots

Figure 6: Signal Frequency : 1498MHz, Sample Frequency 3.0GSPS

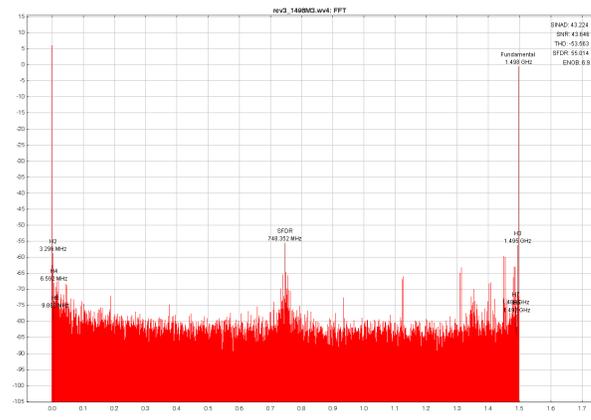
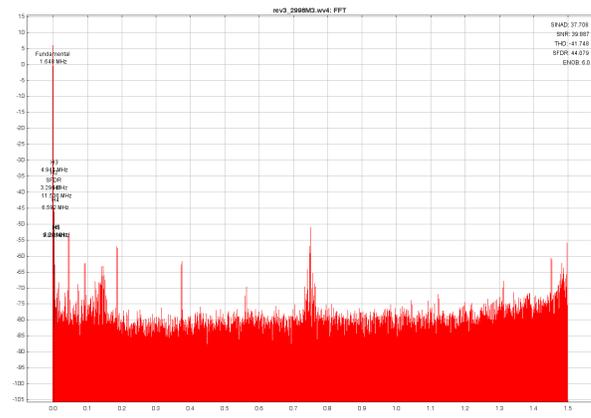


Figure 7: Signal Frequency : 2998MHz (aliased back to ~2MHz) , Sample Frequency 3.0GSPS



### Notes

To gather the results presented here, a spectrally pure sine wave was applied to each input in turn and 16K of data was collected. A 16K FFT was performed and the dynamic parameters were calculated from the FFT. The input signal frequencies were chosen so as to ensure coherent sampling, which removes the need to apply a window function. This allows greater visibility of detail in the FFT, as window functions often hide spurious signals.

For more information on the analog characterization of this product, please contact your local Curtiss-Wright representative for a more complete AD3000 characterization report.



Figure 8: AD3000 Block Diagram

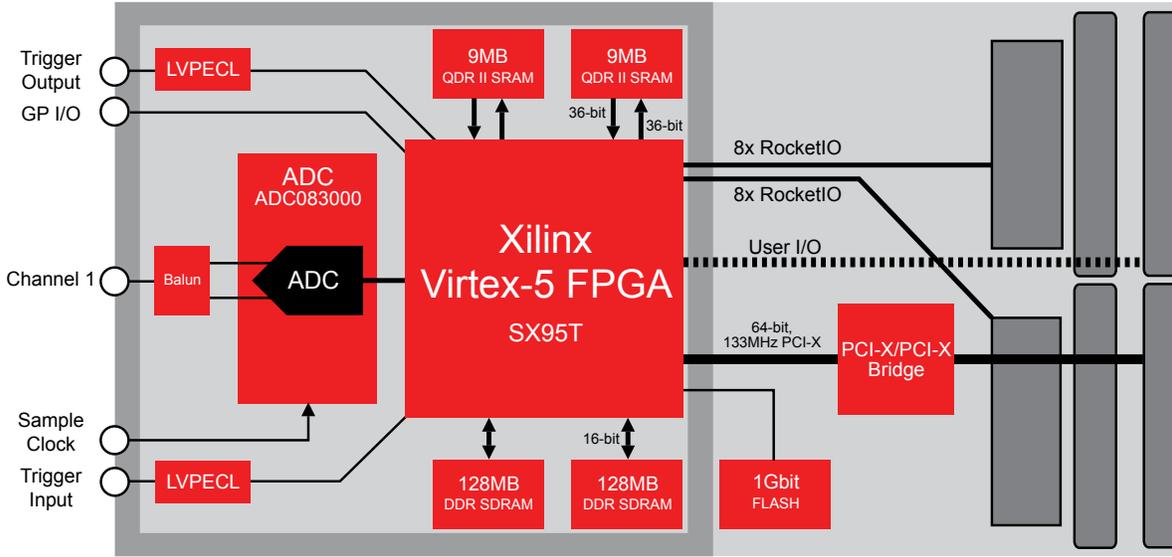


Table 1: Specifications

FPGA	
Device	Xilinx Virtex-5 SX95T (speed grade 2)
DDR2 SDRAM	2 banks of 64M x 16-bit (2 banks of 128MB)
QDR2 SRAM	2 banks of 2M x 36-bit (2 banks of 9MB)
FLASH	1Gbit (FPGA boot/configuration including rescue image)
Analog Input	
Number of Channels	1, single-ended
Sampling Frequency	Up to 3GSPS
Full Scale Input Voltage	600-800 mV (programmable)
Device	ADC083000
Full Power Bandwidth (3dB)	2.2GHz
Input Impedance	50 Ohm, AC coupled
SNR	43.6 dB <sup>1</sup>
SFDR	55.0 dBc <sup>1</sup>
ENOB	6.9-bits <sup>1</sup>
PCI	
PCI Compliance	32/64-bit PCI 33MHz, PCI-X 66/100/133MHz, Master/slave/DMA, Interrupt support

Clock & Trigger Inputs	
External	Front panel MMCX
Input Level	600-1800 mV (sine or square wave)
Input Impedance	50 Ohm, AC coupled
Sample Frequency Range	500MSPS to 3GSPS (uses double edge clock i.e. 1.5GHz clock input for 3GSPS)
Trigger Input/Output	Single-ended, 50 Ohm, LVPECL, DC coupled
XMC	
XMC P15	8x RocketIO @ 3.125GB/s or 8x PCIe
XMC P16	8x RocketIO @ 3.125GB/s
Software/HDL Code	
Host Drivers	Windows, VxWorks 6.x, Linux
Utilities	FLASH programming, diagnostics
Software/HDL Code	Analog input, memory interfaces, PCI-X, PCIe
Miscellaneous	
Weight	Commercial air-cooled 113g Rugged air-cooled 150g Conduction-cooled 141g

Notes

1.  $F_{in} = 1498 \text{ MHz}$ ;  $V_{in} = \text{Full Scale} - 0.5 \text{ dB}$ ;  $F_s = 3000 \text{ MSPS}$   
 All the analog characterizations in this datasheet represent the average measured performance of standard production boards in normal laboratory conditions. These are typical performance figures and are not guaranteed.



**Table 2:**  
**Environmental Specifications**

		Commercial	Rugged	
			Air-cooled	Conduction-cooled
			Level 100 <sup>1</sup>	Level 100 <sup>1</sup>
Temperature	Operational (at sea level)	0°C to +55°C (15 CFM air flow) <sup>2</sup>	-40°C to +70°C (20 CFM air flow) <sup>2</sup>	-40°C to +70°C (Card Edge Temp) <sup>3</sup>
	Non-Operational	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C
Vibration	Operational (Random)	-	0.04g2/Hz	0.1g2/Hz
Shock	Operational	-	30g peak, 11ms half sine	40g peak, 11ms half sine
Humidity	Operational	5-95% non-condensing	Up to 95%	Up to 95%
Altitude <sup>4</sup>	Operational	-	-1,500 to 60,000ft	-1,500 to 60,000ft
Conformal Coating <sup>5</sup>		No	Yes	Yes

**Notes**

1. Availability of the ruggedization levels are subject to qualifications for each product.
2. For operation at altitudes above sea level, the minimum volume flow rate should be adjusted to provide the same mass flow rate as would be provided at sea level. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat. Some higher-powered products may require additional airflow.
3. The contacting surface on the rack/enclosure must be at a lower temperature to account for the thermal resistance between the plug-in unit and rack/enclosure.
4. Depending on the technology used, the risk for Single Event Upsets will increase with altitude.
5. Coated with Humiseal 1B31 or 1B73EPA. (ref. <http://humiseal.com> for details)

\*While the AD3000 is designed to meet these environmental requirements, formal qualification testing has not been performed to these levels. Please contact your local sales representative to discuss your program specific requirements.

**Warranty**

This product has a one year warranty.

**Contact Information**

To find your appropriate sales representative, please visit:

Website: [www.cwcembedded.com/sales](http://www.cwcembedded.com/sales)

Email: [sales@cwembedded.com](mailto:sales@cwembedded.com)

For technical support, please visit:

Website: [www.cwcembedded.com/support1](http://www.cwcembedded.com/support1)

Email: [support1@cwembedded.com](mailto:support1@cwembedded.com)

The information in this document is subject to change without notice and should not be construed as a commitment by Curtiss-Wright Controls Embedded Computing. While reasonable precautions have been taken, Curtiss-Wright Controls assumes no responsibility for any errors that may appear in this document. All products shown or mentioned are trademarks or registered trademarks of their respective owners.