Data Sheet

AD1520

Dual Channel 1.5GSPS Analog Input XMC/PMC

Applications

- Electronic Warfare (EW)
- Electronic Counter Measures (ECM)
- Spectral Analysis
- RADAR

Features

- 2 Channel 1.5GSPS, 8-bit ADC
- Xilinx® Virtex®-5 SX95T FPGA (user programmable)
- Dual banks of QDR2 SRAM and DDR2 SDRAM memories
- Capable of multi-board synchronization
- XMC/PMC form factor
- Air- or conduction-cooled rugged versions
- Windows®, VxWorks® and Linux® support

Benefits

- Combined acquisition and data processing
- Lower power solution
- Industry standard form factor
- PCI Express® provides high throughput to baseboard

Overview

The AD1520 is a second generation 1.5GSPS ADC XMC module and follows on from the AD1500. The AD1520 uses a newer generation ADC device and key benefits include increase full power bandwidth (from 1.5 to over 2GHz) and general improvement in ENOB, SFDR and SNR.

The AD1520 closely couples a high performance Xilinx Virtex-5 FPGA to a dual channel high-speed analog input front end providing both processing and up to 1.5GSPS acquisition (per channel) in a single XMC/PMC card. The combination of a user programmable FPGA, data I/O sub-systems and multiple banks of fast memory provides a powerful platform for acquiring and processing high-speed data in one board. In addition to processing digitized data, the Xilinx Virtex-5 SXT FPGA is used to control the analog to digital converter and provides the off-board interfaces to either PCI-X or the multi-GB/s serial I/O used for the XMC interface.

Analog I/O & FPGA Processing in One

The AD1520 is a combined acquisition and FPGA based data processing module. The majority of the Virtex-5 FPGA resources are available for user programmable processing and are supported by SRAM and SDRAM memories. Some applications that are ideally suited for FPGA based processing include Digital Down Conversion (DDC), Fast Fourier Transforms (FFTs) and digital filters.

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1.5GSPS Analog Input

Analog to digital conversion is performed by a National Semiconductor ADC08D1520 analog to digital converter, which is a dual channel 8-bit, 1.5GSPS device. The analog input stages are transformer AC coupled to the ADC via a balun. Using the ADC's built-in demultiplexer, digitized data is transferred to the FPGA using an interleaved 32-bit interface (2+2 samples in parallel).

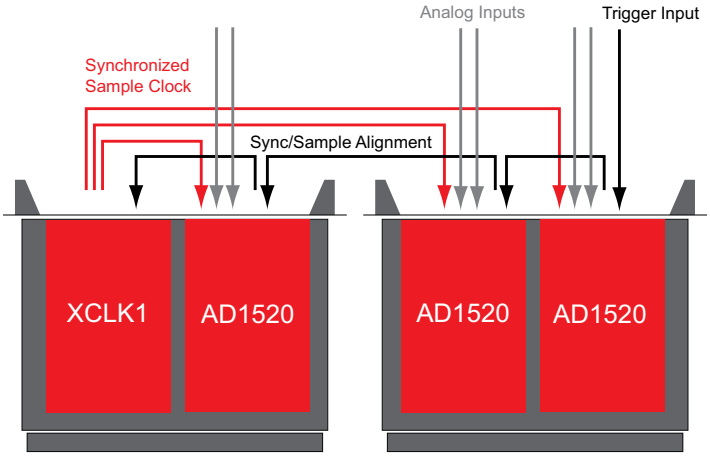
Clocks, Triggers & Multi-board Sync

The AD1520 provides a front-panel MMCX connector for connecting an external sample clock source (required).

A front panel mounted trigger input (TI) and a trigger output (TO) signal are connected to the FPGA via LVPECL I/O stages. This allows the FPGA to define the trigger mechanism in the application for maximum flexibility.

The AD1520 supports multi-board synchronization allowing all ADCs to be synchronized to a common clock source. When synchronized, all data will be aligned and coherent across multiple AD1520 boards. Curtiss-Wright's XCLK1 clock generator is capable of providing this synchronized sample clock output to two or more AD1520 ADCs, providing support for features such as synchronous reset of the sample clock.

Figure 1: Multiple AD1520s can be synchronized



Xilinx Virtex-5 FPGA

The AD1520 is fitted with a Xilinx Virtex-5 SX95T FPGA (contact Curtiss-Wright for availability of other FPGA variants) which is optimized for a high ratio of DSP blocks to standard logic blocks to support high performance signal processing.

The FPGA is configured at power up from FLASH with a default image, a recovery image or an image the customer generates. In addition to FLASH configuration, new images can be downloaded from the host via the PCI or PCI Express (PCIe) interface. Software is provided to load new images into either FLASH or SRAM. Bit streams stored in SRAM benefit from faster downloads while bypassing non-volatile storage - useful for secure applications.

Multiple SDRAM & SRAM Banks

The AD1520 features both external SRAM and SDRAM connected to the FPGA. These can be used for buffering ADC data or for general purpose processing support.

The two 128MB DDR2 SDRAM banks on the AD1520 can be used in parallel to buffer digitized data. Each bank is 16-bits wide.

QDR2 SRAM provides higher bandwidth external memory. Two 2M x 36-bit banks are fitted on the AD1520.



PCI/PCI-X, PCIe & Multi-GB/s I/O

The AD1520 includes a PCI/PCI-X interface, supporting up to 133MHz operation, and a PCIe interface. These interfaces provide multi-channel DMA support.

The PCIe interface uses the Virtex-5 FPGA's RocketIO™ GTP transceivers and an embedded end-point controller, which is a hard IP block within the Virtex-5 FPGA. This built-in PCIe endpoint block supports x4 or x8 lane communications at 2.5GB/s according to the PCIe standard, but can be bypassed to support other protocols like sFPDP or Serial RapidIO® (SRIO). Overall, the Virtex-5 FPGA provides sixteen, full duplex high-speed serial communication links through RocketIO GTP transceivers. These links are evenly split between two XMC (VITA 42) connectors, with each link capable of operation at up to 3.2GB/s and can be driven as independent data streams or bonded to create 'fat pipes' for fewer, but higher bandwidth, data streams.

Rugged Build Options

A range of environmental requirements are addressed by the AD1520: air-cooled benign, air-cooled extended temperature, air-cooled rugged and conduction-cooled. For conduction-cooled applications, the host board must be able to incorporate front panel I/O connections. Depending on the application, a suitable heatsink may be required for conduction-cooled builds.

FusionXF Software/HDL Support

Curtiss-Wright's FusionXF development kit includes software, HDL and utilities with examples and infrastructure for using the AD1520 or the AD3000 on one of Curtiss-Wright's other Xilinx Virtex-5 and Virtex-4 FPGA-based products. FusionXF includes a C-API and sophisticated DMA support.

One of the core elements to the FusionXF development kit is a framework for adding in new IP functionality or capabilities to the FPGA. With support for high-speed DMA capabilities and documented interfaces for the integration of custom IP, FusionXF makes HDL development easier and integration more straightforward.

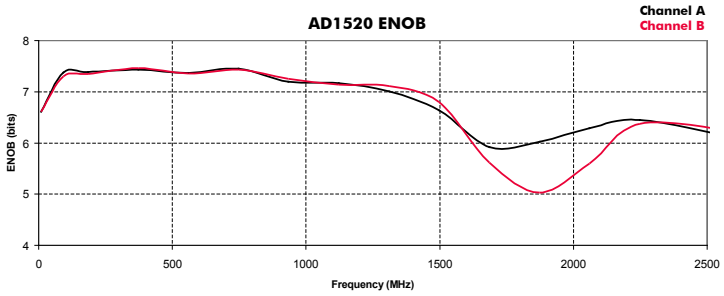
Example software/HDL illustrates how to interface to on-board devices such as QDR SRAM and DDR SDRAM. Under software running on the host, data can be moved to and from the AD1520's memories using FusionXF's high performance DMA capabilities.

Software utilities are provided for configuring the FPGA. These include FLASH programming and commands to configure the FPGA from a given image in FLASH or SRAM. The FPGA may also be configured via a ChipScope™ Pro/JTAG interface. Host operating systems supported by the FusionXF suite includes Windows, VxWorks and Linux. Although the AD1520 is aimed at applications requiring both high-speed digitization and user programmable FPGA processing, a full acquisition-only example image is provided. This allows the AD1520 to be used 'out-of-the-box' without having to develop FPGA code. This image can be loaded from the FLASH file system and supports full bandwidth data acquisition, external trigger modes and high-speed DMA driven PCI-X/PCIe channels to the host processor. This example can be modified to include a user application, making the AD1520 quick and easy to use.



Analog Performance

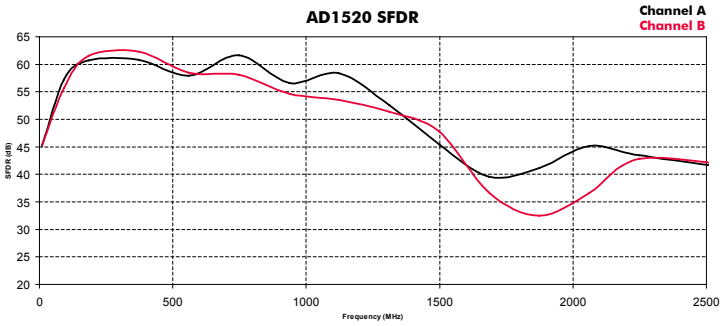
Figure 2: AD1520 Effective Number of Bits



Effective Number of Bits (ENOB)

The AD1520 shows an ENOB greater than 7-bits for the majority of the 1st and 2nd Nyquist zones. This drops below 8MHz and above ~1700MHz. The balun (necessary for wide input bandwidth) at the front end is the primary cause of the low frequency distortion; the high frequency distortion is due in part to the ADC bandwidth and reduced SNR. The AD1520 performance correlates favorably, within 0.2-bits, to the National Semiconductor datasheet for frequencies up to 1500MHz.

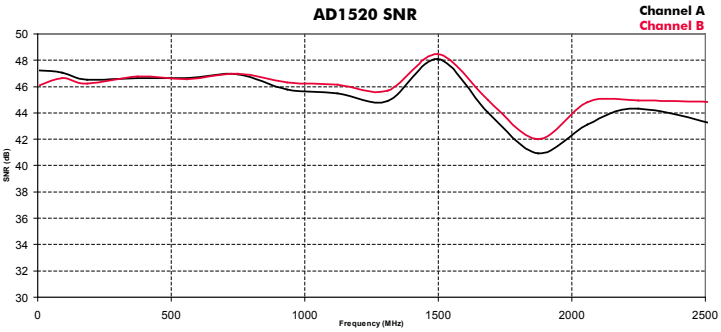
Figure 3: AD1520 Spurious Free Dynamic Range



Spurious Free Dynamic Range (SFDR)

The SFDR is generally dominated by the 2nd or 3rd harmonics of the input signal which are typically introduced by non-linearities in the system. The main non-linear element of the AD1520 is the balun which performs the broadband single-ended to differential signal conversion required for input to the ADC chip. The highest spurious signal is sometimes located at ($F_{Samp}/2$) ± F_{Input}, this spurious signal is caused by the internal folding interpolating architecture of the ADC08D1520 device.

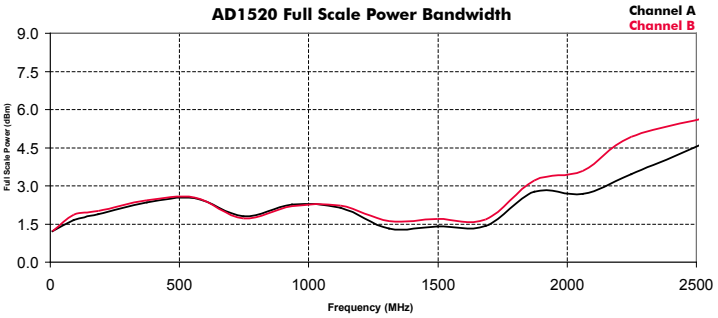
Figure 4: AD1520 Signal to Noise Ratio



Signal to Noise Ratio (SNR)

The AD1520 board exhibits similar characteristics to the ADC08D1520 analog to digital converter, comparing favorably with the National Semiconductor datasheet. The peak SNR is at 1500MHz (vs. approximately 1250MHz in the ADC datasheet) showing an extended performance region of around 200MHz higher than the ADC datasheet

Figure 5: AD1520 Full Scale Power Bandwidth



Gain Bandwidth

The output is normalized to show the input signal level required to give a full scale sampled signal. The AD1520 is shown operating in "Extended Control" mode with the 'Full Scale Voltage Adjust' Register set to 700mVp-p (0.88 dBm). The output shows a 3dB bandwidth approaching 2250MHz (i.e. almost all of 1st, 2nd and 3rd Nyquist regions) with approximately +/- 1dB Gain Flatness in 1st and 2nd Nyquist (0-1500MHz).



Sample FFT Plots

Figure 6: Channel A Signal Frequency: 1310.9MHz (aliased back to ~189MHz), Sample Frequency 1.5GSPS

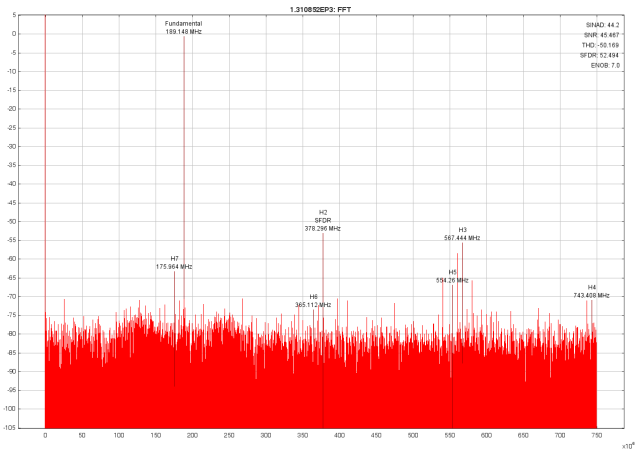
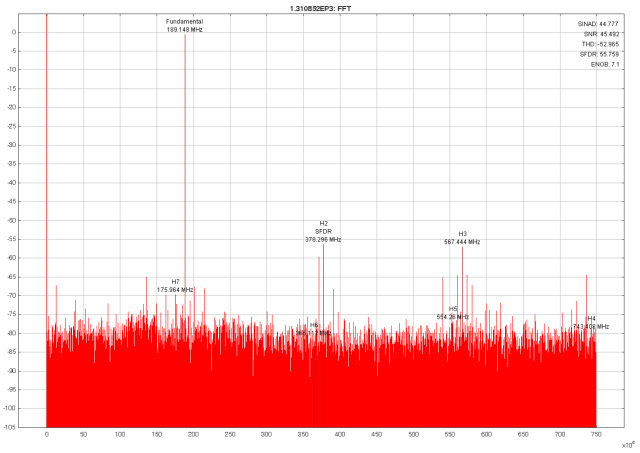


Figure 7: Channel B Signal Frequency: 1310.9MHz (aliased back to ~189MHz), Sample Frequency 1.5GSPS



Notes

To gather the results presented here, a spectrally pure sine wave was applied to each input in turn and 8K of data was collected. An 8K FFT was performed and the dynamic parameters were calculated from the FFT. The input signal frequencies were chosen so as to ensure coherent sampling, which removes the need to apply a window function. This allows greater visibility of detail in the FFT, as window functions often hide spurious signals.

For more information on the analog characterization of this product, please contact your local Curtiss-Wright representative for a more complete AD1520 characterization report.

Figure 8: AD1520 Block Diagram

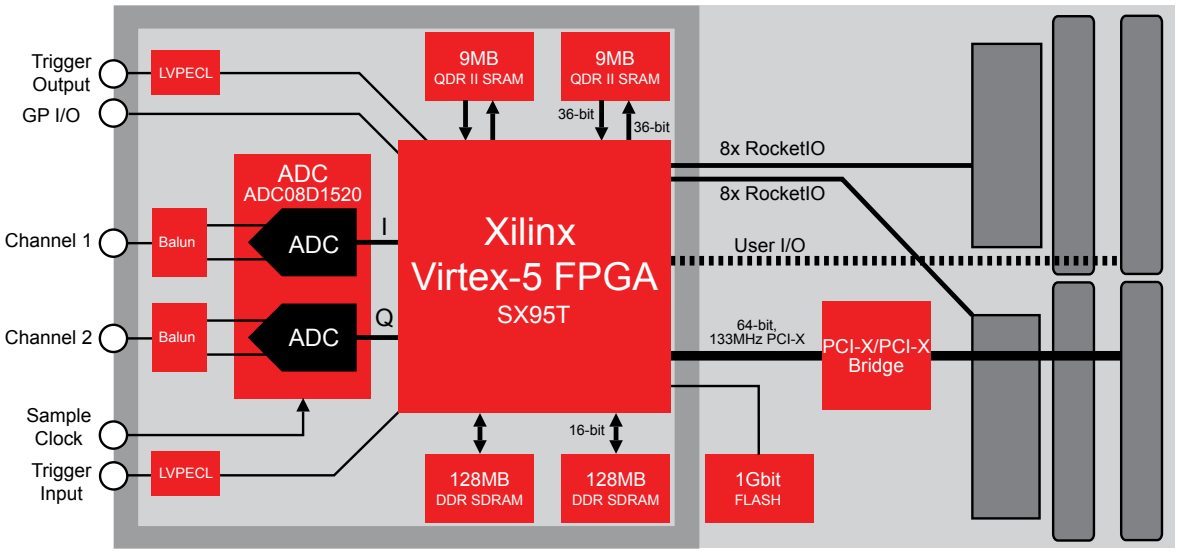


Table 1: Specifications

FPGA	
Device	Xilinx Virtex-5 SX95T (speed grade 2)
DDR2 SDRAM	2 banks of 64M x 16-bit (2 banks of 128MB)
QDR2 SRAM	2 banks of 2M x 36-bit (2 banks of 9MB)
FLASH	1Gbit (FPGA boot/configuration including rescue image)
Analog Input	
Number of Channels	2, single-ended
Sampling Frequency	Up to 1.5GSPS
Full Scale Input Voltage	600-800 mV (programmable)
Device	ADC08D1520
Full Power Bandwidth (3dB)	2.2GHz
Input Impedance	50 Ohm, AC coupled
SNR	46.98 dB[1]
SFDR	61.6 dBc[1]
ENOB	7.45 bits[1]
PCI	
PCI Compliance	32/64-bit PCI 33/66MHz, PCI-X 66/100/133MHz, Master/slave/DMA, Interrupt support

Clock & Trigger Inputs	
External	Front panel MMCX
Input Level	600-1800mV (sine or squarewave)
Sample Frequency Range	200 to 1500MSPS
Input Impedance	50 Ohm, AC coupled
Trigger Input/Output	Single-ended, 50 Ohm, LVPECL, DC coupled
XMC	
XMC P15	8x RocketIO @ 3.125GB/s or 8x PCIe
XMC P16	8x RocketIO @ 3.125GB/s
Software/HDL Code	
Host Drivers	Windows, VxWorks 6.x, Linux
Utilities	FLASH programming, diagnostics
Software/HDL Code	Analog input, memory interfaces, PCI-X, PCIe
Miscellaneous	
Weight	Commercial air-cooled 113g Rugged air-cooled 150g Conduction-cooled 141g

Notes

1. F_{in} = 748 MHz; V_{in} = Full Scale - 0.5 dB; F_s = 1500 MSPS
   All the analog characterizations in this datasheet represent the measured performance of a standard production board in normal laboratory conditions. These are typical performance figures and are not guaranteed.



Table 2:
Environmental Specifications

		Commercial	Rugged	
			Air-cooled	Conduction-cooled
			Level 100[1]	Level 100[1]
Temperature	Operational (at sea level)	0°C to +55°C (15 CFM air flow)[2]	-40°C to +70°C (20 CFM air flow)[2]	-40°C to +70°C (Card Edge Temp)[3]
	Non-Operational	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C
Vibration	Operational (Random)	-	0.04g2/Hz	0.1g2/Hz
Shock	Operational	-	30g peak, 11ms half sine	40g peak, 11ms half sine
Humidity	Operational	5-95% non-condensing	Up to 95%	Up to 95%
Altitude[4]	Operational	-	-1,500 to 60,000ft	-1,500 to 60,000ft
Conformal Coating[5]		No	Yes	Yes

Notes
1. Availability of the ruggedization levels are subject to qualifications for each product.
2. For operation at altitudes above sea level, the minimum volume flow rate should be adjusted to provide the same mass flow rate as would be provided at sea level. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat. Some higher-powered products may require additional airflow.
3. The contacting surface on the rack/enclosure must be at a lower temperature to account for the thermal resistance between the plug-in unit and rack/enclosure.
4. Depending on the technology used, the risk for Single Event Upsets will increase with altitude.
5. Coated with Humiseal 1B31 or 1B73EPA. (ref. http://humiseal.com for details)

*While the AD1520 is designed to meet these environmental requirements, formal qualification testing has not been performed to these levels. Please contact your local sales representative to discuss your program specific requirements.

Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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