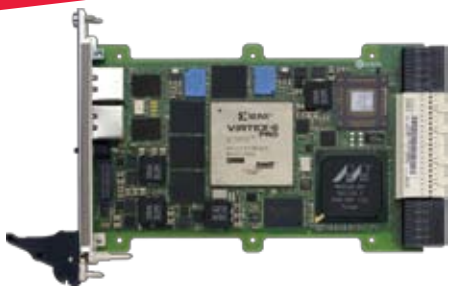
Data Sheet

3CPF1

3U PowerPC/Xilinx Virtex-II Pro Processing Engine



Applications

The 3CPF1 is designed to solve the most demanding scalable processing requirements in embedded systems, in particular for applications such as:

- RADAR
- SONAR
- Electronic warfare / Signal intelligence / Surveillance
- Real-time imaging / EO
- Medical imaging

Features

- 744x PowerPC processor
- Xilinx Virtex-II Pro XC2VP70 FPGA
- 8x Serial I/O links operating up to 3.125Gbps
- High-Speed Ermet ZD connectors for communications channels
- Dual Ethernet to front panel or backplane; RS232 (EIA-232) and RS422 (EIA-422) to backplane
- Independent PowerPC processor and FPGA nodes
- Ruggedized versions available (Air or Conduction cooled)
- VxWorks and Linux support

Benefits

- Tightly coupled FPGA and PowerPC processing nodes
- FPGA connects directly to independent memory banks for maximum flexibility and efficiency in demanding DSP applications

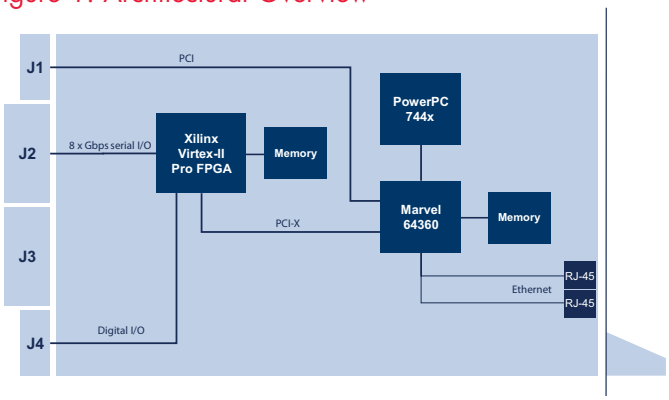
Overview

The 3CPF1 is a modular signal and data processing engine harnessing the combined power of the latest generation of PowerPC CPU, large Xilinx FPGA and high-bandwidth multi-channel serial communications fabric. This creates a balanced and scalable compute platform.

A complete rugged and systems based product philosophy means that the 3CPF1 can be used as a common building block to a range of systems and results in accelerated development cycles and faster time-to-market.

3CPF1 Overview

Figure 1: Architectural Overview



Architecturally, the 3CPF1 consists of two processor nodes; one node is based on the PowerPC 744x CPU and the other node is based on a Xilinx Virtex-II Pro FPGA. Both processor nodes have a fully distributed memory structure with multiple communications channels. The

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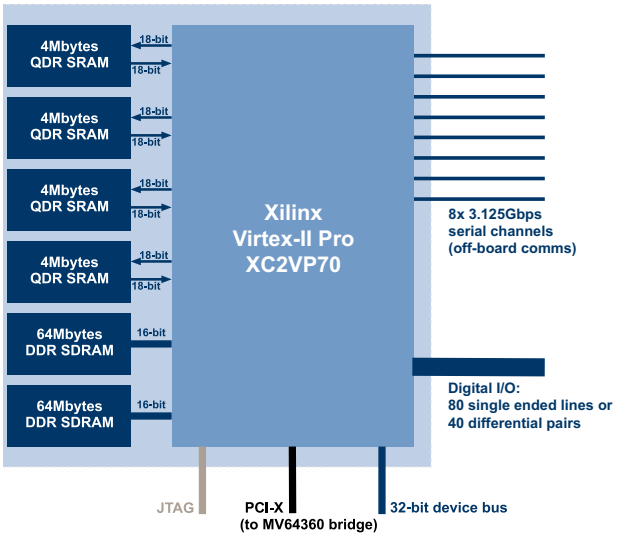
communications fabric connects local processor elements and boards together for a scalable solution.

FPGA Processor Node

Figure 2: FPGA Processing Node



Xilinx Virtex-II Pro FPGA

The 3CPF1's FPGA node is based around a Xilinx Virtex-II Pro XC2VP70 device as standard, though other devices may be fitted: contact Curtiss-Wright for details. Each node features:

- Eight 3.125Gbps SERDES transceiver pairs
- 64-bit/125MHz parallel bus to PowerPC bridge
- Four banks of 2M x 18-bit (4Mbytes) QDR SRAMs
- Two banks of 64/128Mbytes DDR SDRAM

Gigabit Communication Channels

The Virtex-II Pro FPGA features serial communications, via RocketIO™ transceivers, able to operate up to 3.125Gbps. Each RocketIO channel has separate 8/10B encoded LVDS pairs for receive and transmit signals. Groups of RocketIOs from a single device can be 'bonded' together to synthesize fewer, but higher bandwidth data links.

The 3CPF1's high-speed serial communications are electrically compatible with standards such as PCI Express, Serial RapidIO and other switch packet interfaces. The 3CPF1 does not require a protocol to use the card as the FPGA, which drives the high-speed serial interfaces, can also use 'raw' data streams. The use of a communications protocol requires a suitable IP core.

PowerPC Communications

In addition to multi-Gigabit per second serial communications, the FPGA has a fast data-link implemented to the PowerPC node's PCI bridge. This provides a 64-bit/125MHz point-to-point link to the system PCI and the PowerPC 744x's memory.

External FPGA memory - QDR SRAM

The FPGA node includes four banks of 2Mx 18-bit QDR SRAM. QDR memory has the ability to perform read and write operations simultaneously. There are separate read and write busses which clock data on both the rising and falling edge of the clock signal. The QDR memory is clocked at 125MHz, so a bandwidth of 500Mbytes/s, simultaneously for both reads and writes, per device, is available. This provides an aggregate bandwidth of 4Gbytes/s for all four devices. As the QDR SRAM devices are directly controlled by the FPGA, each QDR memory bank can be independently or co-operatively used in various ways such as a FIFO, linear addressable memory pool, bit-reversed addressing or circular buffer as best suits the application.

External FPGA memory - DDR SDRAM

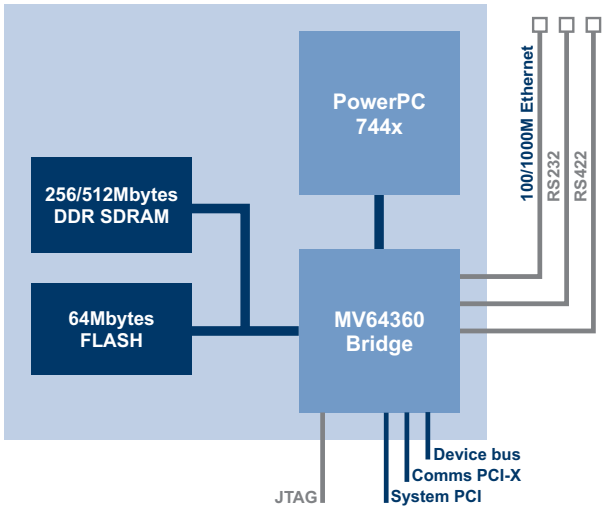
Bulk data storage for the FPGA node is provided via direct FPGA connections to two separate 16-bit wide, 64/128Mbytes DDR SDRAM banks. These memory banks can be used independently or together as a 32-bit wide single bank to store large data-sets such as image frames for medical imaging or temporal processing.

FPGA Configuration

The 3CPF1 FPGA node's configuration is controlled by the PowerPC processor, with the FPGA configuration file being stored in the FLASH. Curtiss-Wright supplies tools for programming the FPGA in both development and run-time environments. The board's JTAG connectivity can also be used for FPGA configuration.

PowerPC Processor Nodes

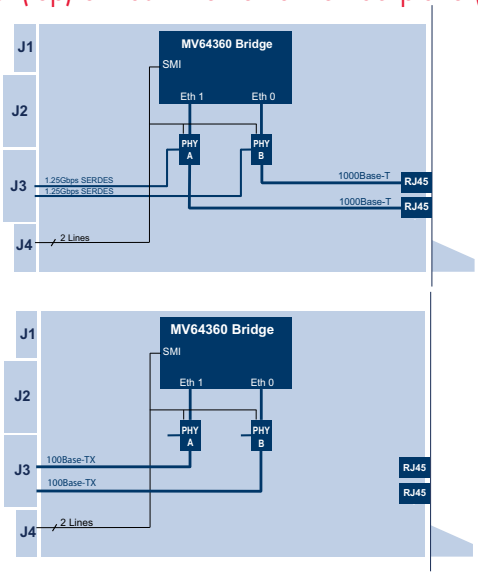
Figure 3: PowerPC Processor Node



The 3CPF1 provides a PowerPC sub-system including a PowerPC 744x with 256/512Mbytes of DDR SDRAM with ECC, coupled via a MV64360 bridge, plus 64Mbytes of FLASH memory. The PowerPC node operates the MPX bus protocol, running at 125MHz with a 64bit data path to give a peak bandwidth of 1GBytes/s. The MV64360 also provides two Gigabit Ethernet channels, RS422/232 ports as well as two PCI/PCI-X interfaces.

Ethernet

Figure 4: 3CPF1 Ethernet options: Gigabit Ethernet to the front panel (top) or Fast Ethernet to the Backplane (bottom)



There are two off-board Ethernet interfaces each providing 10/100/1000Mbit (auto-negotiatiating interface) channels. Both MACs are connected to PHY devices and are available either at the front panel as an RJ45 connection, or at the J3 connector as SERDES.

RS422 (EIA-422) & RS232 (EIA-232) Interfaces

One RS422 interface with RTS/CTS handshaking and one RS232 port is provided by the PowerPC node. The ports are made available to the user through the backplane J4 connector. Both ports are available for user applications and either can be used for a serial console, as required by an operating system bootloader, for boot configuration.

Watchdog Timer

This can be used to cause the board to reset and/or activate an interrupt if the watchdog isn't serviced (reset) by the processor within a pre-defined period of time. This is useful in preventing board 'lock up' in the event of an application failure.

Temperature and Power Monitors

Accessible via the PowerPC processor, the 3CPF1 includes a temperature sensor (controlled via an I^2C bus) to monitor the temperature of the board and the FPGA. The temperature sensor also has an ADC capability that is used to monitor the local supply voltages.

JTAG Interface

The 3CPF1 features multiple, independent JTAG chains via a Firecron JTS01/JTS06 controllers that are accessible via a header near the front panel. The header provides the developer with access to the COP (PowerPC) and ChipScope (FPGA) ports. The separate JTAG chains permit the board to undergo dynamic diagnostics during normal application run-time. A boundary scan debug module is available to allow users to 'break out' these signals to standard debugger connectors.

Input/Output

The 3CPF1 includes a range of high-speed data I/O ports: PCI, multi-channel Gbps serial links, parallel FPGA and Gigabit Ethernet. System I/O such as RS232/422 and JTAG is also supported.

FPGA Parallel I/O

The FPGA has 80 I/O lines directly connected to the J2/J3 connectors. They are routed as 40 differential pairs. As a build option, 2 of the FPGA I/Os (i.e. one pair) may be routed to an FPGA Global clock input which is terminated externally.

Backplane I/O

The majority of input/output for the 3CPF1 is available via the backplane: all the system I/O (such as Ethernet, RS232 and high-speed serial) is routed to the J3 and J4 connectors.

The 3CPF1 has eight, off-board, multi-Gbps transceivers, each of which can be used to establish a point-to-point data link. These links can be wired to create a wide range of topologies to best suite the application such as pipelines of arrays to smoothly scale the system. If more than eight data links are needed, then active switches can be used. These can be implemented within a custom backplane and/or switch card. To supply the bandwidth required by multi-Gigabit data links and Gigabit/fast Ethernet, the J3/J4 connectors of the 3CPF1 are Ermet ZD type connectors with balanced differential signal routing and ground planes. Use of this connector type requires an appropriate customized backplane.

The 3CPF1 employs a high-speed data link (64-bit, 125MHz PCI-X mode) between each PowerPC CPU and one of the FPGAs. The bandwidth afforded by this link (1Gbyte/s) allows the FPGA to be used as a co-processor: data is transferred to the FPGA where one or more IP cores perform compute intensive functions such as FFTs, correlations or imaging warping before the resulting data is returned.

Software and Firmware Support

The 3CPF1 lends itself to different applications and markets. These demands require that the 3CPF1 is available with different layers of software support. For system critical applications, Built-In Test (BIT) provides a power up and run-time system diagnostic. To make application development easier I/O board drivers and optimized libraries are available. The operating systems supported on the 3CPF1 are VxWorks and Linux.

TransComm™

TransComm is a communications toolbox for use with the 3CPF1 and future generation PowerPC and FPGA based products. It is supplied as a set of software and firmware components plus utilities. The package includes a communications harness to facilitate connecting together PowerPC to PowerPC, FPGA to FPGA and FPGA to PowerPC communications for high-performance, low latency data transfer anywhere around the TransComm network - even across bridges. TransComm also allows developers to integrate their own IP within the fabric through the use of simple but well defined interfaces.

This functionality simplifies the process of building and scaling systems by allowing developers to focus on their code development and not worry about the infrastructure. The TransComm toolkit is optional.

Power-On Self Test (POST)

The 3CPF1 architecture includes one PowerPC CPU node with a host bridge incorporating the system memory and FLASH memory controllers, Ethernet controller and bus interfaces. The correct operation of this hardware is critical to the functioning of an operating system (OS) on the board, so the 3CPF1 performs certain POST functions to check that this hardware is in a sound state to facilitate booting an operating system. Checks include:

Memory Checks that the expected amount of memory is available and that all control/address/data lines between the memory controller and memory are intact.

Interrupts Confirms that the interrupt connection between the host bridge and the CPU functions correctly.

Ethernet Checks the connectivity between the Ethernet Media Access Controller (MAC) in the host bridge device, and the Ethernet Physical Layer Device (PHY).

POST tests run automatically at power on and output reports to the console serial port. Upon passing all the tests, the operating system will be booted. In the unlikely event that one or more tests fail, the system will halt. This behavior may be overridden to force operating system boot regardless of test status.

Built In Test (BIT)

Comprehensive testing of the remainder of the system can be carried out using run-time Built-In-Test (BIT) functions, which run in the OS environment of the board. The Curtiss-Wright Built-In-Test system consists of two components: an API and a test specification language. The API allows a BIT script to be run on the hardware. The test specification language provides a precise description of one or more BIT tests for the script.

The specification language contains a series of BIT blocks (see table on opposite page). Each block may be run either sequentially or in parallel. In a sequential block, each BIT test is run in the order listed. In contrast, all tests in a parallel block are started at the same time and rely on the operating system thread scheduler to allocate time on the processor.

BSP Software

To support development, Curtiss-Wright supplies a comprehensive system of BSP software. The major components include user libraries, kernel libraries and utilities.

User Libraries

The Uses Libraries are designed to support general hardware access and high speed DMA transfers. These C++ libraries are source compatible across all supported operating systems. The services provided by the API fall into these broad categories:

- Accessing Remote Nodes
- Allocating DMA Buffers
- Board Initialization
- Bridge Chip SRAM
- Built In Test
- Configuring the FPGA
- DMA Driven I/O
- FLASH Memory
- FRAM Memory
- Hardware Semaphores
- Interrupt Handling
- Persistent Environment Variables
- User Reserved Memory
- Voltage and Temperature Sensors
- Watchdog Timer

Kernel Libraries

The kernel level library includes low level routines required by the VxWorks/Linux kernel in order to run on the 3CPF1 plus a suite of device drivers which enable the kernel and user applications to exploit all available board hardware. The driver suite is divided into two parts: standard (WindRiver/Linux and Marvell) device drivers and Curtiss-Wright 3CPF1 specific drivers. The low level access to operating system functionality means these library functions are not portable between supported operating systems.

Most Curtiss-Wright library routines return an error code. Macros are provided to manipulate these error codes, aiding in application debugging.

Utilities

Board Viewer Tool:
Provides snapshot access to all of the registers (including user defined FPGA registers) and most of the memory on a Curtiss-Wright card. BView is a client/server program, with a graphical user interface (GUI) running on a Windows 2000/XP PC and a monitor daemon running on the 3CPF1 card.

Xilinx Configuration Utility:
Configures the FPGA either from a host file or from data already stored in the node's FLASH memory.

Card Environment Access Utility:
Provides access to the system and user environment variables stored in a node's FLASH memory. System environment variables describe a card's build properties (e.g. clock speeds, amount of memory fitted, etc.), while user environment variables can be used for any application purpose.

FLASH Viewing and Programming Utility:
Allows the user to reserve regions of FLASH to be programmed with application data, including bootable kernels, FPGA configuration data and BIT scripts.

The BSP includes a number of example programs showing how to use the APIs for numerous essential tasks such as setting up DMAs, handling interrupts, running BIT, setting up a watchdog, etc.

Figure 5: 3CPF1 Adapter Module

Figure 6: 3CPF1 Adapter Module Block Diagram

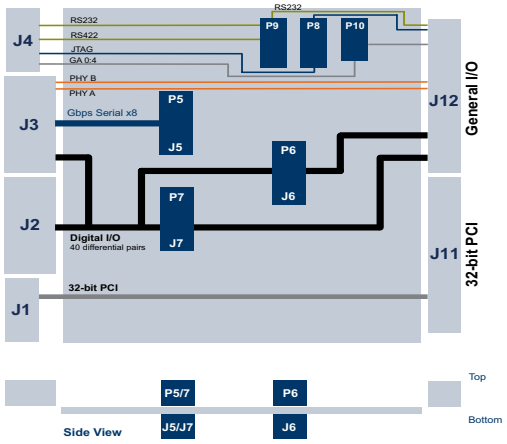
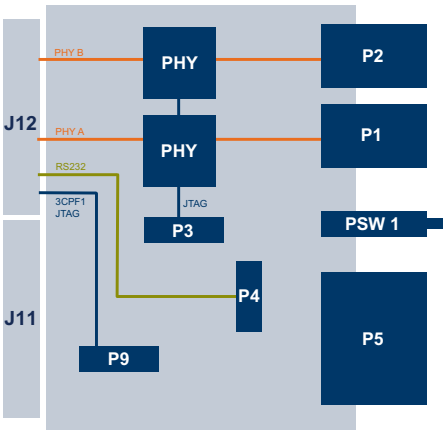


Table 1: Built In Test (BIT) Functionality

Test	Description
DDR Byte Write	Confirms that byte writes to the DDR memory attached to the FPGA are functional
DDR Refresh	Confirms that the DDR memory attached to the FPGA is being properly refreshed
DDR/QDR Data Generator/ Checker	Confirms that the data checkers and generators in the FPGA memory interface correctly generate & check their defined test data patterns
DDR/QDR DMA	Confirms that the FPGA can reliably transfer test data to and from an attached memory device
DDR/QDR Independence	Confirms individual memory devices may be accessed without interfering with each other
DDR/QDR Size	Confirms that the expected amount of memory is connected to the FPGA and available for use
Error Reporter	Generates errors to validate the error reporting system
Flash	Confirms that the flash can be read
FRAM	Confirms that a defined region of FRAM memory is writable and readable
JTAG Controller	Confirms that the controller is accessible from the host
Marvell Integrity Monitor	Hooks all the Marvell integrity interrupts (e.g. bus parity errors) and redirects them into the BIT test report
Network Error Monitor	Monitors for transmit and receive errors on a specified ethernet interface
Network Load	Connects a client to a specified server, and sends a specified count of packets of given size
Network Load Server	Starts a server on a specified interface, waits (with timeout) for a client connection and sinks any data received
PCI Bus Master Abort	Confirms that the bridge chip receives a master abort for invalid PCI cycles
PCI-X DMA checker	Confirms that the data checkers and generators in the FPGA's PCI-X interface correctly generate and check their defined test data patterns
PCI-X DMA Input/Output	Confirms that the bridge can reliably transfer test data between the FPGA & PowerPC SDRAM over the PCI-X bus
POST Results	Evaluate the results of POST tests run before the OS booted
Power Dissipation	Determines the level of power dissipated by the test firmware's power block
QDR DCM Sweep	Sweep the QDR Digital Clock Manager over its full frequency range
QDR Parity	Confirms that parity error detection for the QDR memory is operational
Real Time Clock	Confirms that the RTC is incrementing
RocketIO Data Checker	Confirms that the data checkers and generators in the FPGA RocketIO interface correctly generate & check their defined test data patterns
RocketIO Data transfer	Confirms that the FPGA can reliably send data through a specified RocketIO link
Simple Worker	Provides a variable CPU load, so that the BIT control system can be validated
Synchronous QDR	Confirms that the FPGA can simultaneously transfer test data reliably to/from all QDR memory devices
System Clock	Confirms that all system clocks are running at the correct frequency
System Voltage	Confirms that the boards power supply rails are within 5% of nominal values
Temperature alarm	Confirms that the temperature sensors correctly detect defined alarm conditions
Temperature Monitor	Periodically prints out board temperatures
Voltage Monitor	Periodically prints out board voltages
Watchdog Alarm	Confirms that the watchdog can be enabled and serviced
Xilinx Configuration	Confirms that the FPGA can be deconfigured and that the test firmware can then be configured into the device
Xilinx Integrity Monitor	Hooks all the Xilinx integrity interrupts (e.g. QDR parity errors) and redirects them into the BIT test report
Xilinx Interrupt	Confirms that the FPGA is able to generate interrupts to the bridge chip
Xilinx Register	Confirms that the FPGA generates the correct 'bus ready' signal on the register bus
Xilinx Register Bus Parity	Confirms that the bridge chip receives correct parity on the FPGA device bus

Figure 7: 3CPF1 Transition Module

Figure 8: 3CPF1 Transition Module Block Diagram



Firmware Development Support

In a number of instances, the services provided by the BSP are dependent on the functionality of the firmware configured into the FPGA. In order to ensure compatibility between user defined firmware and the BSP, Curtiss-Wright supplies a number of standardized firmware interface components and recommends that a set of "standard" registers are implemented in the FPGA by users. A "features" register defines which elements are actually implemented. The firmware library components include:

Functional interface components

- DDR SDRAM interfaces
- Device bus interface
- ICS8442 programming interface
- PCI-X interface
- QDR SRAM interface

Simulation model components

- DDR SDRAM simulation model
- MV64360 bridge simulation model
- QDR SRAM simulation model

Other library files

- Component definitions for all library components
- Constants and types definitions
- ModelSim Macro file for library compilation
- ModelSim project file
- Text file revision history of the library files section
- Utilities used by the MV64360 simulation

3CPF1 Adapter Module

The 3CPF1 uses high-speed connectors in the J2 and J3 positions rather than the standard CompactPCI connectors. Curtiss-Wright supplies the 3CPF1 Adapter Card which converts the 3CPF1 connectors to standard 32bit 3U CompactPCI pinout and also allows stand-alone operation of the 3CPF1. This adapter enables developers to evaluate the 3CPF1 in a standard cPCI chassis. It is available in two variants - one for system slot usage and one for peripheral slot usage.

Routing

Standard 32-bit PCI maps straight through to J11, whereas RocketIO signals are broken out through high speed Samtec connectors at P5 and J5. These connectors are on opposite sides of the board, with P5 on the top side and J5 in the bottom. The routing is set so that boards in adjacent slots can link directly: i.e. the transmitter pin of a RocketIO in P5 maps to the receiver pin of the same RocketIO on J5 of the adjacent board.

The 40 User I/O differential pairs are routed so as to prevent contention at power up. Each differential pair on P6/7 is mapped to a neighboring pair on J6/7. For example user I/O pairs 18 and 16 are adjacent on P6. When connected to the adjacent board J6, the first board's pair 18 maps to the second board's pair 16, while the first board's pair 16 maps to the second board's pair 18. The same signals are also routed onto the cPCI backplane User I/O pins.

Ethernet signals are routed through for backplane signaling or for breakout using the transition module.

3CPF1 Transition Module

The 3CPF1 Transition Module can only be used in conjunction with a 3CPF1 Adaptor Card. The Transition Module allows access to the backplane Ethernet connections from the 3CPF1 (either SERDES or raw 100Mbit) and to the RS232 serial link and JTAG port.

Routing

The Ethernet signals are routed to PHYs and on to the rear RJ45 connectors P1 and P2. The PHYs are controlled remotely from the 3CPF1 card. There is a JTAG port for the PHY devices.

RS232 signals are routed to P4 and on to the 9 way D-type connector P5. 3CPF1 JTAG can be accessed from P9.

3PF1 Debug Module

The 3CPF1 connects all debug signals to a single connector near the front panel. A debug breakout module is available for developers to access these signals. There is a COP port connector on the debug module for the PowerPC processor. Xilinx FPGA JTAG ports are provided to allow JTAG configuration and chipscope debugging of the FPGA.

Figure 9: Air and conduction cooled 3CPF1 boards

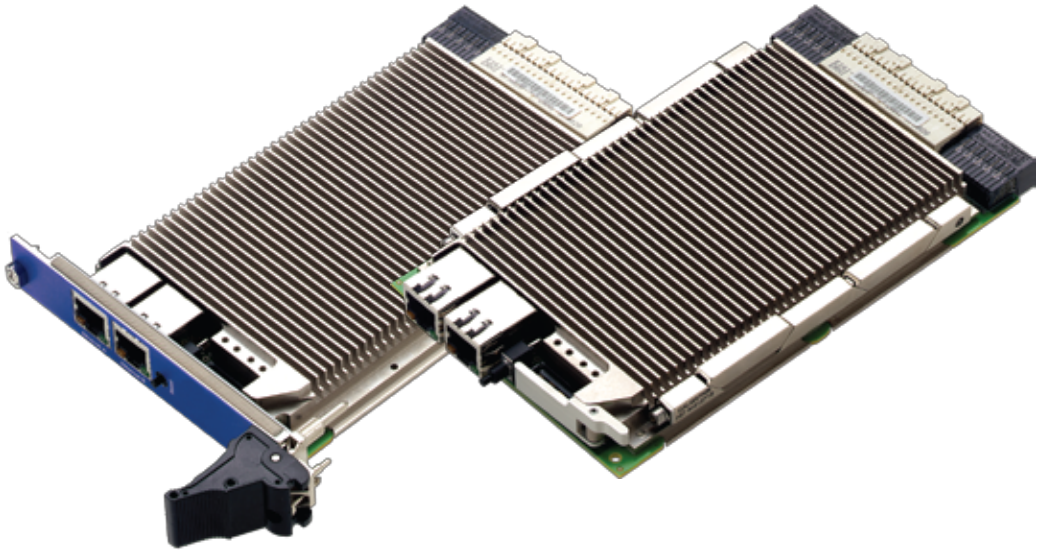




Table 2: Specifications

PowerPC Node	
Number	1
Processor	PowerPC 7447 1000MHz PowerPC 7447A 1000MHz* PowerPC 7448 1250MHz*
Bridge	Marvell MV64360
SDRAM	256 or 512 (future) Mbytes DDR SDRAM with ECC
FLASH	64 Mbytes
Ethernet	100Base-T 1000Base-T
Serial I/O	1x RS232 (EIA-232) 1x RS422 (EIA-422)
FPGA Node	
Number	1
FPGA	Xilinx Virtex-II Pro XC2VP70
Serial I/O	RocketIO up to 3.125 Gbps
QDR SRAM	4 banks of 2 or 4 Mbytes 18-bit datapaths
SDRAM	128 Mbytes (2 banks of 64 Mbytes) with ECC 16-bit data paths

Debug	
JTAG	Multiple JTAG/COP chains - Front panel adapter or backplane
Backplane Adapters	
3CPF1 Adapter, System Slot	3CPF1 to standard 3U connector conversion for system board
3CPF1 Adapter, Peripheral Slot	3CPF1 to standard 3U connector conversion for peripheral board
3CPF1 Transition	Backplane signal break-out
Software Support	
Operating Systems (PowerPC)	VxWorks, Linux
Diagnostics	POST, BIT
Libraries	User, Kernel
Firmware	Interface & Simulation components

* Please consult Curtiss-Wright for 7447A and 7448 device availability

Ruggedized versions

Curtiss-Wright offers ruggedized versions of the 3CPF1 that are characterized for extended temperature range, shock, vibration, altitude and humidity. These boards are equipped with extra and/or special hardware to improve tolerance against shock and vibration.

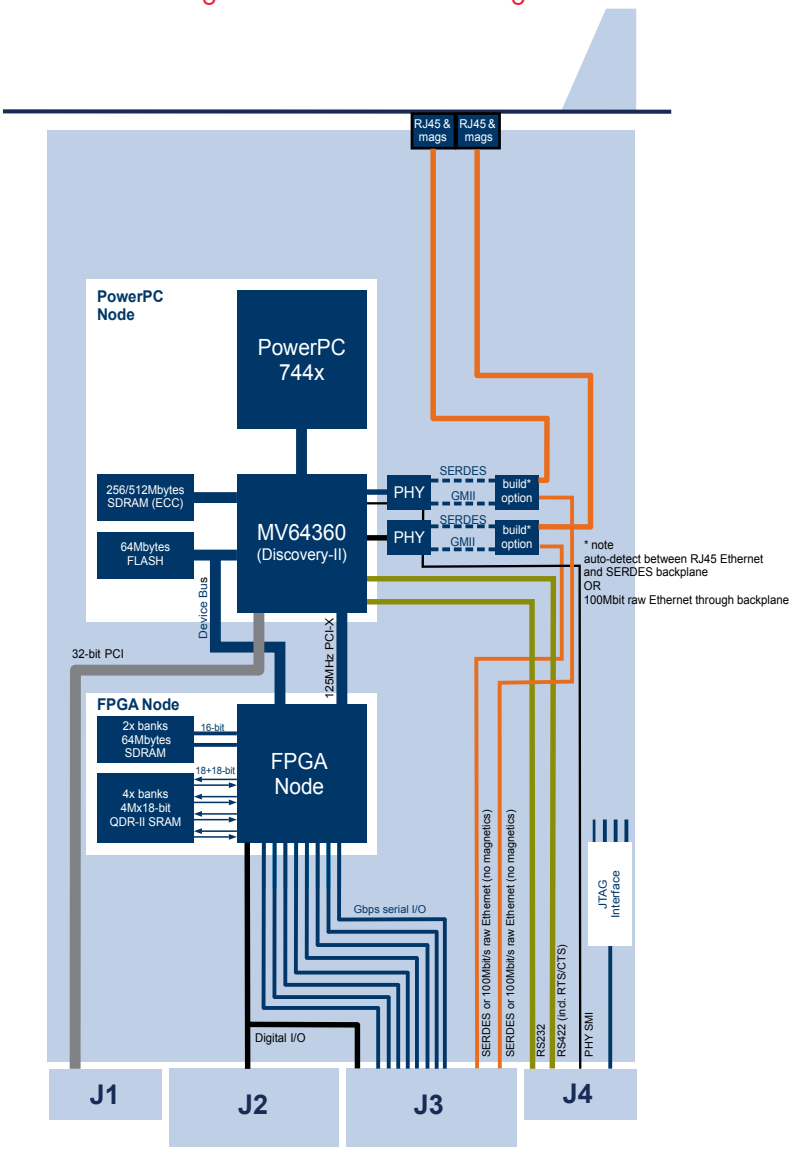
Table 3: Environmental Specifications

Part number extension		Air Cooled		Conduction
		Level 1	Level 2	Level 4
Temperature	Operational[1] (at sea level)	0°C to 50°C Inlet 8 cfm air flow at sea level	-10°C to 65°C Inlet 8 cfm air flow at sea level	-40°C to 75°C Card edge temperature
	Non-operational	-40°C to 85°C	-40°C to 85°C	-55°C to 85°C
Vibration	Operational (Sinus)	-	-	10G peak 15-2000Hz
	Operational (Random)	-	0.02 g^2/Hz (20-2000Hz)	0.04 g^2/Hz (15-2000Hz)
Shock	Operational	-	30 g peak 11ms half sine	40 g peak 11ms half sine
Humidity	Operational non-condensing	0-95% non-condensing	0-95% non-condensing	0-100% non-condensing
Altitude	Operational	10,000 ft	20,000 ft	70,000 ft
Conformal Coat		No	Yes	Yes

Notes

1. The maximum operating temperature is heavily dependant on the power dissipation of the FPGA devices: Applications with high levels of FPGA utilization may not operate to the maximum ambient temperatures stated. The maximum temperature figures given here are for a 3CPF1 where the FPGA is operating with a power dissipation of 20W.

Figure 10: 3CPF1 Block Diagram



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative, please visit:

Website: www.cwcembedded.com/sales

Email: sales@cwcembedded.com

For technical support, please visit:

Website: www.cwcembedded.com/support1

Email: support1@cwcembedded.com

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