VPX3-663

Hybrid PCI® and 10G Ethernet Switch with XMC

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Key Features

- Hybrid PCIe and 10G Ethernet Switch
  - 6F6U and 6F8U profile options for OpenVPX systems and systems aligned with the SOSA™ Technical Standard
- PCIe 3.1 data or expansion plane switch with 24 lanes to the VPX backplane
- Flexible PCIe configuration supporting x8, x4, and x2 links
  - Up to six separate root partitions for multi-host applications
  - Non-transparent bridging (NTB) available for any ports supporting host-to-host communications
- 10G Ethernet control plane switch
  - Up to 8 ports of 10GBASE-KR
  - Up to 2 ports 1000BASE-T
  - 2 ports SFP+ on front panel of air-cooled modules
- XMC site for hosting PCIe-connected mezzanine
  - Ideal for expansion using storage, GPU, or FPGA co-processors without I/O requirements
  - Can also support an Ethernet routing, network services, or security mezzanine

Applications

- Single-slot connectivity for next-generation mission systems that combine SBC, DSP, GPU, FPGA, and I/O modules
- High-performance PCIe fabric for 3U multi-processing clusters

SOSA Sensor Open Systems Architecture MEMBER

Overview

The VPX3-663 from Curtiss-Wright combines a PCI Express® (PCIe) Gen3 switch and a 10G Ethernet switch into a single 3U VPX module. It provides a versatile building block for a variety of processing systems requiring high-performance and flexible connectivity in size, weight, and power (SWaP)-constrained platforms.

The VPX3-663 features a 32-lane PCIe 3.1 switch, supporting a wide range of flexible PCIe expansion and connection topologies. When used for simple PCIe expansion, a single host module (root) can support up to 11 downstream modules such as I/O, GPU, and FPGA devices. Ports can be configured with 2-lane, 4-lane, or 8-lane widths and support PCIe Gen1 (2.5GT/s), Gen2 (5GT/s) and Gen3 (8GT/s) speeds.

The PCIe switch supports multiple partitions, with different hosts (PCIe roots) connecting independently to downstream ports, and also provides a powerful non-transparent bridging capability (NTB) between hosts. This enables multiple hosts to share a resource such as a GPU or to make possible direct communication between hosts across the PCIe fabric. For PCIe inter-processor communication, the VPX3-663 is supported by our Dolphin eXpressWare PCIe fabric software, available on many Curtiss-Wright SBC and DSP modules.

An XMC mezzanine site is available to mount PCIe connected modules, offering a zero-slot expansion capability for connected hosts.

To complement the PCIe switch, the VPX3-663 includes an independent 10 Gigabit Ethernet switch, with up to eight 10GBASE-KR and up to two 1000BASE-T interfaces to the backplane. Two additional SFP+ ports are available on the front of air-cooled modules. The Ethernet switch supports a wide range of multi-layer (L2+) networking features for managing traffic and enforcing security policies. Ethernet network management is supported in-band via CLI, web and SNMP, as well as an out-of-band serial port.

When designing systems that combine commercial off-the-shelf (COTS) modules, interoperability can present significant challenges. The VPX3-663 is available to match the OpenVPX switch profiles of 6F6U and 6F8U and is compatible with common off-the-shelf development backplanes. Variants are also available aligned with The Open Group Sensor Open Systems Architecture™ (SOSA) Technical Standard.

The VPX3-663 has been validated for interoperability with a wide range of Curtiss-Wright modules, enabling rapid system development.

Designed for superior durability and reliability, the VPX3-663 incorporates Curtiss-Wright's industry-leading hardware and software design and validation practices to meet the stringent requirements of the most demanding front-line environments.

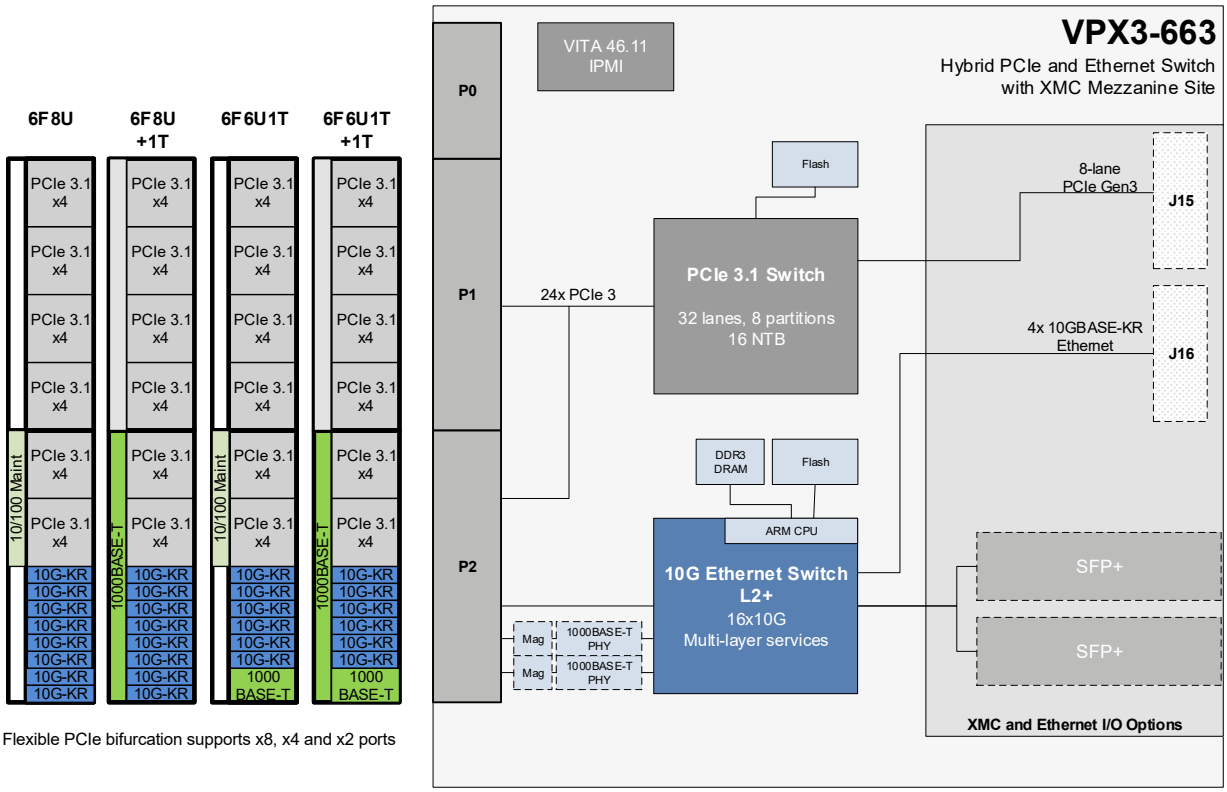

Figure 1: VPX3-663 Hybrid PCIe and 10G Ethernet Switch

Specifications

Form factor

- 3U VPX – VITA 65 OpenVPX, supporting module profiles:
  - MOD3-SWH-6F8U-16.4.10, SLT3-SWH-14.4.9
  - MOD3-SWH-6F6U-16.4.1, SLT3-SWH-14.4.1

PCI Express EP or DP Switch

- Non-blocking PCIe 3.1 switching
  - Supports PCIe Gen1 (2.5 GT/s), Gen2 (5.0 GT/s) and Gen3 (8.0 GT/s) interface speeds
- 24 lanes of PCIe to the backplane
  - Flexible bifurcation of PCIe links with 8-lane, 4-lane and 2-lane ports
- Up to 16 non-transparent bridges (NTB) assignable to any port

XMC Mezzanine Site

- 8-lane PCIe interface to PCIe switch
- Assignable to any connected PCIe host (root)
- Supports Gen1, Gen2 and Gen3 interface speeds
  - Standard VITA 42 connector supports Gen1, Gen2 and Gen3 speeds
  - VITA 61 connector available for enhanced signal integrity at Gen3 speeds
- J16 I/O is not available on the backplane. J16 connector is not populated on standard variants
- XMC site can support an Ethernet processing mezzanine with J16 connectivity to the 10G Ethernet switch. Contact factory for details.
- Thermal qualification with 25 watt mezzanine

PCIe Fabric Communications Software

- Compatible with Curtiss-Wright's Dolphin eXpressWare PCIe Fabric Communications Library software
- Supports high-speed, low latency data fabric communications between SBC and DSP processing nodes
- Also supports PCIe peripheral sharing and lending, for use with PCIe connected processing resources such as GPU and FPGA modules

Ethernet Control Plane Switch

- Six or eight ports of 10GBASE-KR backplane Ethernet
  - 10GBASE-KR ports auto-negotiate to 1Gbps to support 1000Base-KX link partners
- Up to two 1000BASE-T ports for standard twisted-pair interfaces
- Two SFP+ interfaces are available on front panel of air-cooled modules
  - For lab development, supports copper 1000BASE-T, 10GBASE-SR optical, and passive copper (DAC) cabling
  - Note: SFP+ modules not supported for variants with XMC mezzanine site

Multi-Layer Ethernet services

- IEEE 802.1d bridging with support for STP, RSTP, MSTP
- VLANs and IEEE 802.1q tagging
- Link aggregation per 802.3ad and LACP
- IP multicast via IGMP, MLD snooping
- QoS and ACLs based on L2-L4 headers
- Multiple queues per port; priority queueing
- Rate limiting and flexible scheduling

Ethernet Access Control & Port Security

- Port-based authentication via IEEE 802.1x
- MAC-based access control lists
- DHCP snooping
- Static MAC filtering
- ACLs based on L2-L4

Ethernet Timing Services

- IEEE 1588-2008 Precision Time Protocol (PTPv2) transparent clock

Management Interfaces

- Command-line interface (CLI) for configuration and monitoring via RS-232 serial console
- In-band management over Ethernet interfaces
  - SSH, SNMP, or Web interface
  - HTTP and HTTPs for configuration and SW update
- Independent 10/100 Mbps management Ethernet port for software upgrades

Health Management

- IPMC per VITA 46.11 for all Tier 1 and Tier 2 requirements

Serviceability & Monitoring

- Power-up BIT (PBIT)
- User Initiated BIT (IBIT)
- Continuous BIT (CBIT)

Power

- Primary Power: factory orderable as Vs1 (+12V) or Vs3 (+5V) main power
- Typical power consumption = 15-20 watts
- Maximum power consumption = 26 watts

Environmental

- Air-cooled: available in Level 0 and Level 100
  - Air-cooled pitch = 1.0"
- Conduction-cooled: available in Level 200 and Level 300
  - L200 pitch = 0.8" without XMC installed
  - L200 pitch = 1.0" with XMC installed
  - L300 pitch = 1.0" with or without XMC installed
- VITA 48.8 Air Flow-Through also available

Weight

- Air-cooled Level 0, 100: 320 g
- Conduction-cooled Level 200: 355 g
- Conduction-cooled Level 300: 425 g

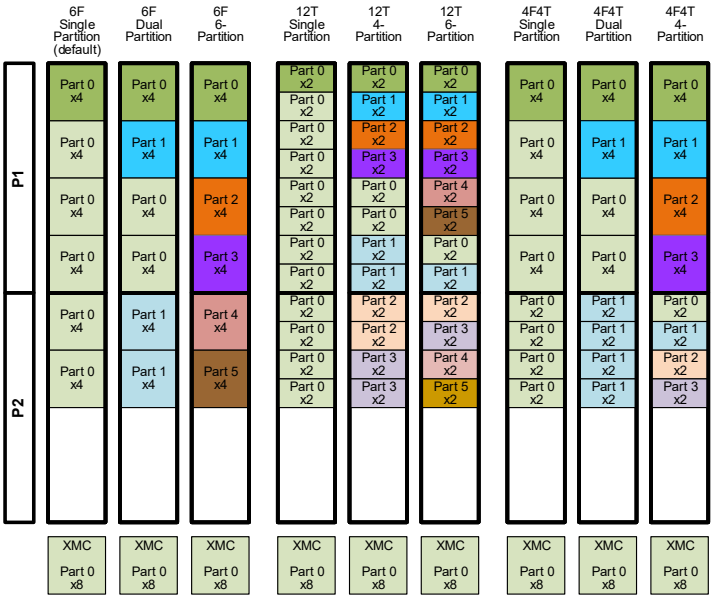

Figure 2: PCIe Standard Switch Configurations

PCIe Switching

Flexible PCIe Architectures

PCI Express is a point-to-point connection between a root node (host) and a downstream device. The VPX3-663 is designed to provide flexible PCIe expansion, with one or more hosts connected to one or more downstream devices. With 24 available PCIe lanes, and offering ports with lane widths from 2-lane to 8-lane, the VPX3-663 can be configured to support almost every possible PCIe architecture.

Using the VPX3-663, a PCI architecture with a single root node, typically an SBC or DSP processor, can connect to many downstream devices. All downstream devices become part of the root node's PCI addressable bus.

A system can also be architected with two or more separate PCI buses, or partitions, allowing independent SBC hosts to connect to dedicated sets of downstream devices. The VPX3-663 supports multiple partitions, with up to six independent hosts connected to their set of downstream devices.

Figure 2 illustrates a number of standard configurations available on the VPX3-663 PCIe switch. For each partition, the darker color is the root/host node, and the lighter colors are downstream connections.

Additional configurations can be created to support unique architectures. Contact Curtiss-Wright for more details.

Figure 3 shows an example system with a single host processor connected to two downstream peripheral or I/O modules. Figure 4 shows the same example system with downstream GPU and an FPGA modules. Both examples use 8-lane PCIe connections. Figure 5 shows a similar 8-lane host processor connected to four downstream 4-lane devices.

The PCIe standard allows devices to auto-negotiate lane widths, for example, allowing a downstream 1-lane PCIe device to connect to a single lane of an upstream 4-lane or 8-lane PCIe connection. Similarly a downstream 8-lane PCIe device can connect to an upstream 4-lane PCIe connection.

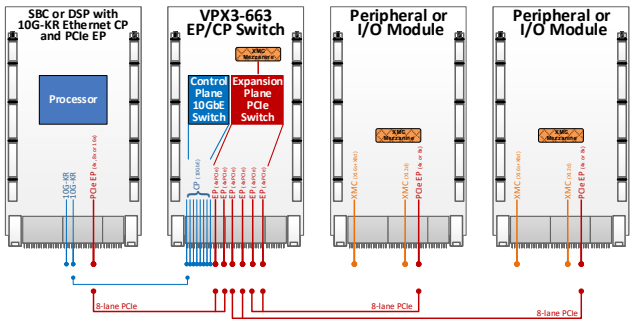

Figure 3: Single 8-lane PCIe Host Connected to Two 8-lane Downstream Peripheral I/O Modules

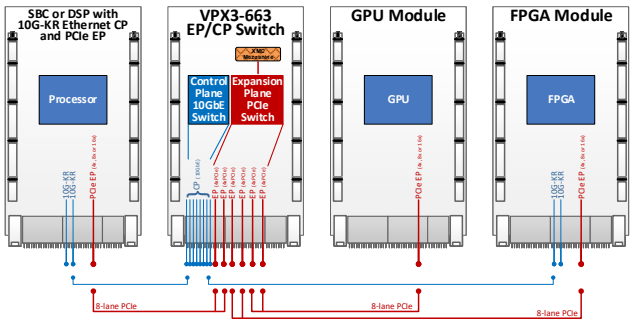

Figure 4: Single 8-lane PCIe Host Connected to Two 8-lane Downstream Devices: GPU and FPGA

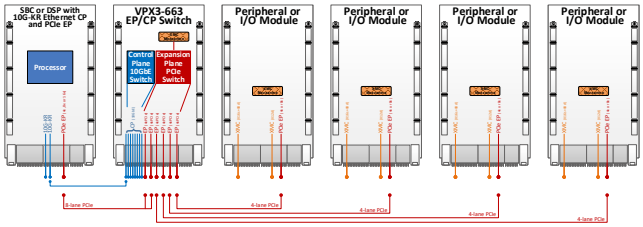

Figure 5: Single 8-lane PCIe Host Connected to Four 4-lane Downstream Devices

XMC Mezzanine

The VPX3-663 supports a single XMC mezzanine module connected to the PCIe switch. An 8-lane PCIe connection provides the highest possible interface width, and the PCIe switch is configured to connect the XMC mezzanine to the first PCIe partition or host.

The XMC site supports PCIe interface speeds of Gen1 (2.5 GT/s), Gen2 (5.0 GT/s), and Gen3 (8.0 GT/s). Standard VPX3-663 modules utilize VITA 42 connectors for maximum compatibility, and VITA 61 connectors are also available for enhanced Gen3 signal integrity.

As all VPX backplane pins are assigned for use as PCIe and Ethernet signals, the VPX3-663 does not provide the XMC Mezzanine with backplane I/O. As such, the mezzanine site does not populate Pn6. Front panel I/O is supported on air-cooled modules.

The following are some examples where the VPX3-663's XMC mezzanine site can provide powerful zero-slot expansion capabilities to VPX systems:

- Add an SSD storage mezzanine to expand the non-volatile data storage capacity of a connected host
- Add a GPGPU mezzanine as a processing resource to one or more hosts
- Add an FPGA mezzanine as a processing or security resource, or using front panel I/O for sensor ingest

Note that the XMC mezzanine is not supported on air-cooled variants equipped with front panel SFP+ slots.

Dolphin PCIe eXpressWare Fabric Software

Curtiss-Wright has partnered with Dolphin Interconnect Solutions to provide a PCI Express Fabric Communications Library for SBC and DSP modules supporting high-speed, low-latency peer-to-peer communications using direct PCIe connections. This software library hides the complexities and technical details of programming directly to PCIe devices, and presents an easy to use software API to application developers wishing to send high-speed messages and bulk data between computing nodes.

The VPX3-663 can be used with Dolphin eXpressWare to create powerful central switch PCIe architecture systems. Figure 6 illustrates a three processor system configured with 8-lane PCIe connections to the VPX3-663 central switch. Using the Dolphin eXpressWare fabric software, the processors can communicate across this high-speed 64Gbps interface.

Figure 7 shows a similar central switch configuration with six processors connected with 4-lane PCIe connections supporting 32Gbps interface speeds. A mixed configuration is also possible, such as some nodes connected with 8-lane and other nodes connected with 4-lane connections.

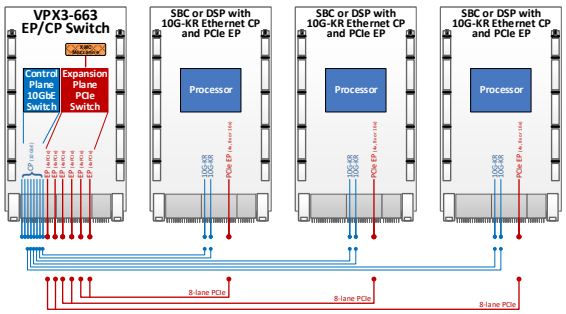

Figure 6: Three Processors Connected to VPX3-663 Central Switch with 8-lane PCIe Connections and 10GbE Control Plane

PCIe Device Lending and Sharing

The Dolphin eXpressWare software also permits PCIe peripheral sharing. Peripheral sharing allows one processor to own a PCIe connected resource, such as

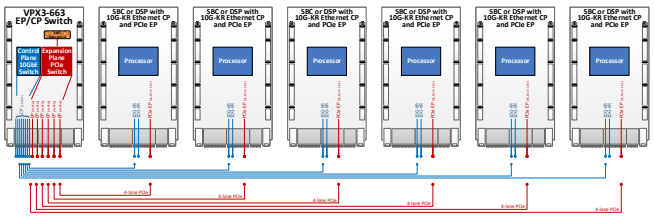

Figure 7: Six Processors Connected to VPX3-663 Central Switch with 4-lane PCIe Connections and 10GbE Control Plane

an FPGA or GPU, and then share this resource to other processing nodes.

Figure 8 illustrates a system where two processing nodes can share a GPU or FPGA resource. In this example, the shared resource is another VPX module connected by PCIe to the VPX3-663 central switch. Dolphin software runs on the SBC/DSP processing nodes.

Figure 9 shows a variation of this sharing mechanism where three processors can share an XMC mezzanine peripheral mounted on the VPX3-663. In this example, the shared XMC mezzanine GPU does not consume a VPX slot.

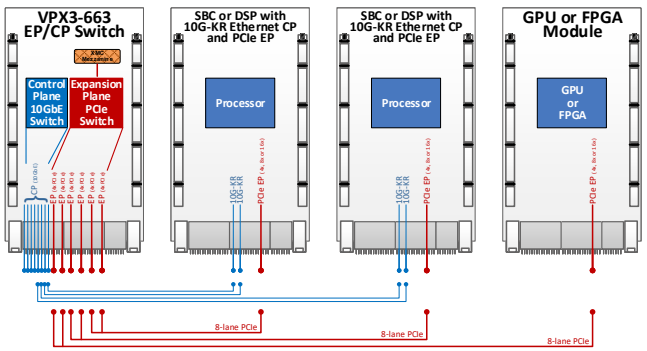

Figure 8: Perpheral Sharing of a 3U VPX FPGA or GPU

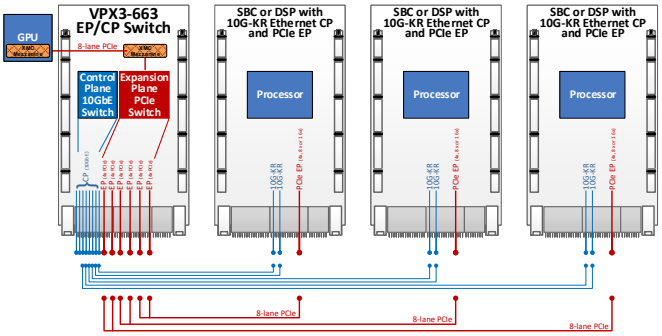

Figure 9: Perpheral Sharing of an XMC FPGA or GPU Mounted on the VPX3-663

Ethernet Switching Features

To connect between VPX modules and to external systems, the VPX3-663 features up to 9 ports of standards-based Gigabit Ethernet supporting 1G and 10G connection speeds.

All models offer backplane (SerDes) Ethernet ports, supporting 10GBASE-KR interfaces,and feature auto-negotiation compatible with 1000BASE-KX link partners.

Up to two 1000BASE-T ports are also supported for internal backplane connections or for robust external connections using low-cost twisted-pair cabling. The 1000BASE-T ports offer auto-negotiation with 100BASE-TX and 10BASE-T partners for legacy 10/100Mbps interfaces.

The quantity and types of Ethernet ports is factory configured at order time. The following four configurations are available and are identified by the VPX profile nomenclature at the top of Figure 10 (6F8U, 6F8U+1T, 6F6U1T, 6F6U1T+1T).

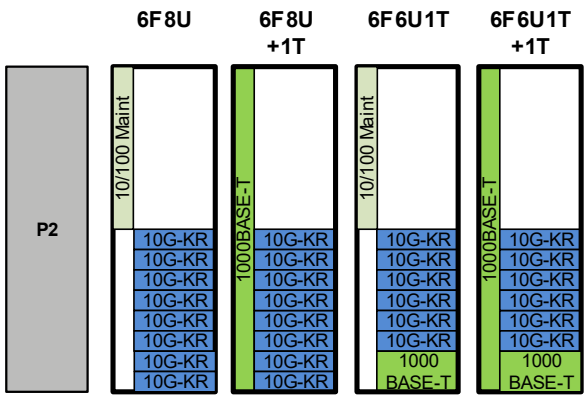

Figure 10: Factory Orderable Ethernet Port Configurations

High-Performance Ethernet Switching

The VPX3-663 features an energy-efficient switching core that provides line-rate, non-blocking forwarding for all packet sizes in all configurations. It performs extensive packet processing in hardware to provide an array of features at full rate without performance degradation.

Powerful Layer 2 Networking Features

In today's embedded systems, a switch must provide more than connectivity – it must ensure secure and reliable forwarding for a variety of applications on a converged network.

Managed networking software integrated on the VPX3-663 provides a rich set of enterprise-class multi-layer switching features. Policy features such as VLANs and Access Control Lists (ACLs) allow traffic to be filtered and segregated. Support for IGMP snooping allows multicast traffic to be efficiently forwarded. Flexible quality of service (QoS) mechanisms can classify traffic to provide priority forwarding to delay-sensitive real-time applications. Port security and 802.1x authentication restrict access to the network to trusted devices.

Secure Management Interfaces

As embedded computers transition from stand-alone appliances to connected systems, the importance of network security continues to grow. The VPX3-663 is designed with cyber-security in mind and uses a number of approaches to limit and mitigate potential vulnerabilities.

To support both system development and stable deployment, VPX3-663 offers multiple management interfaces for configuring and monitoring its networking features. These administrative interfaces can be individually disabled to limit access, protected with passwords, or secured with standards-based encryption. Hardware write protection features can be used to prevent unauthorized or unintentional modification of the switch configuration. Logging of configuration changes and administrative actions facilitates security audits. Other network services exposed on the switch interfaces can be disabled to further limit potential network threats.

Software Maintenance

To keep pace with emerging requirements and security threats, Curtiss-Wright continues to maintain switch networking software over the full life-cycle of a product. Customers with an active support contract receive access to periodic updates that address potential vulnerabilities and maintain compliance with published specifications.

Time and Synchronization

Maintaining accurate time is essential for many applications, including those that combine data from multiple sensors or connected systems. To enable high-precision synchronization of real-time clocks over the Ethernet network, the VPX3-663 supports the IEEE 1588-2008 Precision Time Protocol. Acting as a transparent clock, the module uses hardware timestamps in the switch to account for the transit time through the network, allowing connected endpoints to synchronize with sub-microsecond precision.

QoS and Real-Time Networking

Capable of forwarding at line-rate on all interfaces, the VPX3-663 delivers high performance and low latency packet switching for applications with high data rates. For applications where multiple applications share the network, a variety of quality of service (QoS) mechanisms are available to manage congestion and prioritize time-sensitive flows. Hardware parsing allows classification of packets based on L2-L4 headers. Multiple output queues per port and configurable queue service schemes enable low-latency treatment for high-priority traffic. Rate limiting can be used to police best-effort traffic to enforce partitioning of overall network bandwidth.

Reliability and Serviceability

The VPX3-663 features a comprehensive power-on built-in test (PBIT) suite to detect hardware faults that affect module performance. Additional tests can be initiated (IBIT) while the card is operational.

To support diagnostics and monitoring at the system level, interface status and operating statistics (CBIT) are available via the management Command Line Interface (CLI). These vital signs can also be monitored using an array of SNMP MIBs.

Front Panel Ethernet Ports

Air-cooled variants of the VPX3-663 are available with two SFP+ module slots accessible on the front panel. These slots provide additional system flexibility in both lab development and deployed environments and support a range of commercial plug-in modules to support copper and optical interfaces.

The front panel SFP+ slots are not supported on air-cooled variants configured with an XMC mezzanine site.

NOTE: While SFP+ plug-in modules are available for extended temperature operation, Curtiss-Wright does not recommend using SFP+ module slots for rugged environments subject to shock and vibration conditions.

XMC Mezzanine as an Ethernet Security Processor

The VPX3-663's XMC mezzanine site supports the addition of the Pn6 I/O connector, with dedicated 10G Ethernet connections to the Ethernet switch.

This architecture allows a custom XMC mezzanine module to extend the functionality of the VPX3-663's Ethernet subsystem.

Examples of additional functionality include:

- Network routing and traffic management, supporting standard routing protocols as well as mission-critical radio-aware and mobile ad-hoc routing for voice, video and data communications
- DHCP and similar network services
- VLAN trunking
- Secure connectivity services such as VPN
- IPsec and Suite-B cryptography support

For additional details on Ethernet mezzanine features and availability, please contact Curtiss-Wright.

Designed for Harsh Environments

Curtiss-Wright modules are designed and manufactured to meet the challenging requirements of military, aerospace and industrial environments and benefit from decades of experience and investment focused on achieving the highest levels of quality and durability.

The VPX3-663 is available in Curtiss-Wright standard L0, L100 and L200 ruggedization levels.

Accessories for Development

To facilitate system development, the VPX3-663 rear transition module (RTM3-663) provides access to the serial management console and maintenance interfaces on convenient lab-friendly connectors.

PCIe and Ethernet ports are not available on the RTM. These high-speed signal integrity sensitive signals should be routed between modules across the VPX backplane.

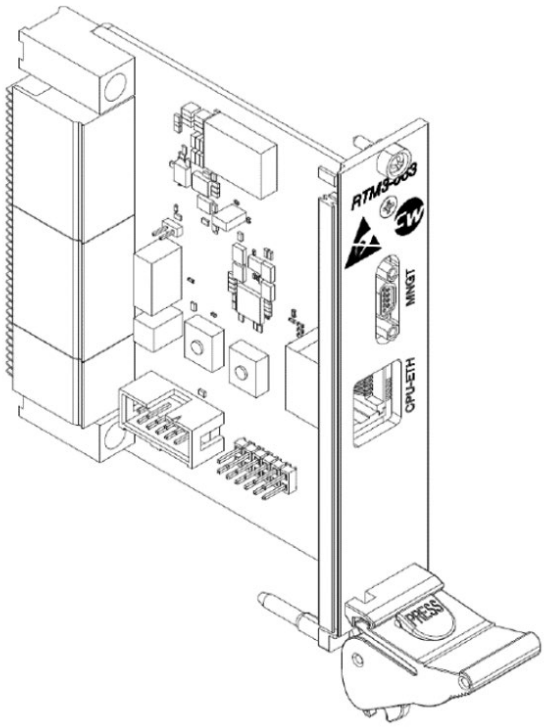

Figure 11: RTM-663 Rear Transition Module

Ordering Information

The VPX3-663 is ordered with the following part number convention. Not all possible configurations are offered – see Standard Ordering Configurations below or contact Curtiss-Wright for additional configurations.

TABLE 1

PART NUMBER	DESCRIPTION
VPX3-663-A04wxyz	Air-cooled Level 0, 0 to +50°C, 1.0” pitch front panel and metalwork
VPX3-663-A14wxyz	Air-cooled Level 100, -40 to +50°C, 1.0” pitch front panel and metalwork
VPX3-663-C21wxyz	Conduction-cooled Level 200, -40 to +85°C card edge, 0.8” pitch without XMC installed, 1.0” pitch with XMC installed
w	Power Options › 1: Vs1 (+12V) main power › 5: Vs3 (+5V) main power
x	I/O Options › 1: No XMC, front panel RS-232 on mDB9, dual SFP+ › 2: XMC Pn5 with VITA42 connector, no front panel RS-232 or SFP+ › 3: XMC Pn5 with VITA61 connector, no front panel RS-232 or SFP+ › 4: XMC Ethernet processing mezzanine (Pn5 and Pn6 installed) (VITA61)
y	Backplane Ethernet Configuration › 0: 6F8U, dual 10G-KR on P2w15-16, 10/100 Mgmt on P2SE › 1: 6F8U+1T, dual 10G-KR on P2w15-16, 1000BASE-T Fabric on P2SE › 2: 6F6U1T, 1000BASE-T on P2w15-16, 10/100 Mgmt on P2SE › 3: 6F6U1T+1T, 1000BASE-T on P2w15-16, 1000BASE-T Fabric on P2SE › 5: 6F8U+1T SOSA Aligned, dual 10G-KR on P2w15-16, 1000BASE-T Fabric on P2SE, LVTTL serial port
z	PCIe Switch Configuration › 0: default configurations per data sheet, user configurable

Standard Ordering Configurations

The following VPX3-663 module combinations are available as standard variants.

TABLE 2 Standard Ordering Configurations

ETHERNET PORT CONFIGURATION				
RUGGEDIZATION & ADDITIONAL FEATURES	6F8U (Y = 0)	6F8U+1T (Y = 1)	6F6U1T (Y = 2)	6F6U1T+1T (Y = 3)
AC-L0, dual SFP+ (x=1)	VPX3-663-A04w100	VPX3-663-A04w110	VPX3-663-A04w120	
AC-L0, XMC Mezzanine (x=2)		VPX3-663-A04w210	VPX3-663-A04x220	VPX3-663-A04w230
AC-L100, dual SFP+ (x=1)	VPX3-663-A14w100	VPX3-663-A14w110	VPX3-663-A14w120	
AC-L100, XMC Mezzanine (x=2)			VPX3-663-A14x220	VPX3-663-A14w230
CC-L200, XMC Mezzanine (x=2)	VPX3-663-C21w200		VPX3-663-C21w220	VPX3-663-C21w230
CC-L300, XMC Mezzanine (x=2)				VPX3-663-C25w230
CC-L300, XMC Mezzanine, SOSA-Aligned Pinout (x=2, y=5)	n/a	VPX3-663-C251250	n/a	n/a

Variant digit ‘w’: substitute 1 for Vs1 (+12V) main power, or 5 for Vs3 (+5V) main power

TABLE 3

PART NUMBER	SOFTWARE AND ACCESSORIES
RTM3-663-010	Management Rear Transition Module for VPX3-663 › Provides breakout connectors for serial RS-232 and 10/100 Ethernet management ports (VPX3-663 variants 6F8U and 6F6U1T only) › Includes one CBL-663-FPL-000 to convert mDB9 to standard DB9 › Passive module – does not require Vs1 or Vs3 power
RTM3-663-120	Management Rear Transition Module for VPX3-663, LVTTL Serial Port › Provides breakout connectors for serial RS-232 and 10/100 Ethernet management ports (VPX3-663 variants 6F8U and 6F6U1T only) › Includes one CBL-663-FPL-000 to convert mDB9 to standard DB9 › Converts LVTTL serial port to RS-232 levels › Vs1 (+12V) backplane power required
MNT-663-0001	VPX3-663 annual switch software maintenance › Provides access to regular software updates, including fixes and feature enhancements
SVC-663-CFG	VPX3-663 Custom PCIe Configuration Service › Custom PCIe switch configuration service
CBL-663-0000	VPX3-663 Back-Entry 100BaseTX Ethernet cable
CBL-663-FPL-000	VPX3-663 Front Panel micro-DB9 to standard DB9 serial cable adapter